EE4802: VLSI CIRCUIT DESIGN

Effective Term
Semester A 2022/23

Part I Course Overview

Course Title
VLSI Circuit Design

Subject Code
EE - Electrical Engineering
Course Number
4802

Academic Unit
Electrical Engineering (EE)

College/School
College of Engineering (EG)

Course Duration
One Semester

Credit Units
3

Level
B1, B2, B3, B4 - Bachelor's Degree

Medium of Instruction
English

Medium of Assessment
English

Prerequisites
EE2000 Logic Circuit Design

Precursors
Nil

Equivalent Courses
Nil

Exclusive Courses
Nil

Part II Course Details

Abstract

This course is aimed at providing students with an understanding of Digital VLSI Circuit design as well as provide exposure to the CAD software used in the digital IC design industry through hands-on projects.

Course Intended Learning Outcomes (CILOs)

	CILOs	Weighting (if app.)	DEC-A1	DEC-A2	DEC-A3
1	Describe different logic design circuit families		x	x	
2	Describe different memory cells and peripheral circuits		x	x	
3	Understand the methodologies for design automation of digital VLSI Integrated circuits		x	x	
4	Utilize this knowledge to design a digital IC such as neural network VLSI Design for AI		x	x	x

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to real-life problems.

A3: Accomplishments
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

Teaching and Learning Activities (TLAs)

	TLAs	Brief Description	CILO No.	Hours/week (if applicable)
1	Lecture	Students are taught the fundamental principles to design and analyze digital VLSI logic and memory circuits in typical IC process. Key concepts are clarified and reinforced based on problems.	1, 2, 3	3 hrs/week
2	Laboratory	Students will have laboratory session to practice the learnt concepts in designing digital integrated circuits using Industry standard CAD software	2, 3, 4	3 hrs/week (5 weeks)

Assessment Tasks / Activities (ATs)

	ATs	CILO No.	Weighting (%)	Remarks (e.g. Parameter for GenAI use)
1	Tests(min.: 2)	1, 2, 3	30	
2	#Assignments (min.: 3)	1, 2, 3	30	1 take home assignment
3	Lab Exercises/Reports			2 Lab reports

Continuous Assessment (%)

60

Examination (%)

40

Examination Duration (Hours)

2.5

Additional Information for ATs

Remark:
To pass the course, students are required to achieve at least 30% in the coursework and 30% in the examination. Also, 75% laboratory attendance rate must be obtained.

may include homework, tutorial exercise, project/mini-project, presentation, lab report

Assessment Rubrics (AR)

Assessment Task

Examination

Criterion

Achievements in CILOs

Excellent (A+, A, A-)

High

Good (B+, B, B-)

Significant

Fair (C+, C, C-)

Moderate

Marginal (D)

Basic

Failure (F)

Not even reaching marginal levels

Assessment Task

Coursework

Criterion

Achievements in CILOs

Excellent (A+, A, A-)
High

Good (B+, B, B-)
Significant

Fair (C+, C, C-)
Moderate

Marginal (D)
Basic

Failure (F)
Not even reaching marginal levels

Part III Other Information

Keyword Syllabus

Introduction to VLSI systems
CMOS IC fabrication process; Feature sizes, System complexity; Automated design methods

Logic circuits
CMOS; Dynamic logic; Domino; Dual-rail differential logic

Memory circuits
DRAM; SRAM; Flash; In-memory computing

VHDL Refresher

Logic Synthesis & Physical Synthesis

Placement and Routing (P&R)

Technology Mapping

Simulation and Verification
Functional verification; testbench; Test pattern generation, boundary scan-chains; fault simulation and testing; timing analysis, formal verification

Reading List

Compulsory Readings

	Title
1	Nil

Additional Readings

	Title
1	J. M. Rabaey, A. Chandrakasan and B. Nikolic: Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson, 2003
2	R. Jacob Baker: CMOS: Circuit Design, Layout, and Simulation, 4th edition, Wiley-IEEE Press, 2019.
3	Ken M. Martin: Digital Integrated Circuit Design, Oxford University Press, 1999.
4	John P. Uyemura: CMOS Logic Circuit Design, Springer, 2001.