City University of Hong Kong
Course Syllabus

offered by Department of Electrical Engineering
with effect from Semester A in 2021/2022

Part I Course Overview

Course Title:	Logic Circuit Design
Course Code:	EE2000
Course Duration:	One Semester (13 weeks)
Credit Units:	3
Level:	B2
Proposed Area: *(for GE courses only)*	☐ Arts and Humanities ☐ Study of Societies, Social and Business Organisations ☐ Science and Technology
Medium of Instruction:	English
Medium of Assessment:	English
Prerequisites: *(Course Code and Title)*	EE1001 Foundations of Digital Techniques
Precursors: *(Course Code and Title)*	Nil
Equivalent Courses: *(Course Code and Title)*	Nil
Exclusive Courses: *(Course Code and Title)*	Nil

Part II Course Details

1. Abstract

The aim is to provide students with an understanding of the concepts and design of logic circuits, including (i) various devices, techniques for analyzing and designing combinational circuits and sequential circuits, circuit design and implementation techniques, and (ii) Hardware Description Language (HDL) modelling and synthesis of combinational and synchronous sequential circuit, circuit implementation with FPGA devices. The electrical characteristics of selected logic families are also covered.

2. Course Intended Learning Outcomes (CILOs)

(CILOs state what the student is expected to be able to do at the end of the course according to a given standard of performance.)

No.	CILOs[#]	Weighting* (if applicable)	Discovery-enriched curriculum related learning outcomes (please tick where appropriate)		
			A1	*A2*	*A3*
1.	Apply different methods to simplify combinational logic functions and sequential machines			√	
2.	Analyze and design combinational and synchronous sequential circuits		√	√	
3.	Identify electrical characteristics of different logic families		√	√	
4.	Design logic circuit using VHDL Hardware Description Language		√	√	
5.	Implement logic circuits with Xilinx FPGA		√	√	
6.	Apply basic theories to practical work		√	√	
		100%			

** If weighting is assigned to CILOs, they should add up to 100%.*

[#] Please specify the alignment of CILOs to the Gateway Education Programme Intended Learning outcomes (PILOs) in Section A of Annex.

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to self-life problems.

A3: *Accomplishments*
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

3. Teaching and Learning Activities (TLAs)

(TLAs designed to facilitate students' achievement of the CILOs.)

TLA	Brief Description	CILO No.						Hours/week (if applicable)
		1	2	3	4	5		
Lecture	Explain keys concepts such as binary code, logic circuit, combinational and sequential circuit.	√	√	√	√	√		3 hours/week

Tutorial	Discuss and practice how to use the lecture materials in real implementations through the tutorial questions.	√	√	√	√	√		1 hour/week
Laboratory	Identify, design, and apply the fundamental logic circuits to practical work using Hardware Description Language (VHDL) and Xilinx FPGA chip.	√	√	√	√	√		3 hours/week for 5 weeks

4. Assessment Tasks/Activities (ATs)

(ATs are designed to assess how well the students achieve the CILOs.)

Assessment Tasks/Activities	CILO No.						Weighting*	Remarks
	1	2	3	4	5	6		
Continuous Assessment: 50%								
Tests (min.: 2)	✓	✓	✓	✓		✓	30%	
#Assignments (min.: 3)	✓	✓	✓	✓		✓	10%	
Lab Exercises/Reports				✓	✓	✓	10%	
Examination: 50% (duration: 2hrs								
Examination	✓	✓		✓		✓	50%	
** The weightings should add up to 100%.*							100%	

Remark:

To pass the course, students are required to achieve at least 30% in course work and 30% in the examination. Also, 75% laboratory attendance rate must be obtained.

may include homework, tutorial exercise, project/mini-project, presentation

5. Assessment Rubrics

(Grading of student achievements is based on student performance in assessment tasks/activities with the following rubrics.)

Assessment Task	Criterion	Excellent (A+, A, A-)	Good (B+, B, B-)	Fair (C+, C, C-)	Marginal (D)	Failure (F)
1. Examination	Achievements in CILOs	High	Significant	Moderate	Basic	Not even reaching marginal levels
2. Coursework	Achievements in CILOs	High	Significant	Moderate	Basic	Not even reaching marginal levels

6. Constructive Alignment with Major Outcomes

Please state how the course contribute to the specific MILO(s)

MILO	How the course contribute to the specific MILO(s)
1	An ability to apply knowledge of mathematics, science and engineering.
2	An ability to design and conduct experiments as well as to analyse and interpret data.
3	An ability to design a system, component.
5	An ability to identify, evaluate, formulate and solve engineering problems.
7	An ability to communicate effectively.
10	An ability to use necessary engineering tools.

Part III Other Information (more details can be provided separately in the teaching plan)

1. Keyword Syllabus

Revision of Boolean algebra

Boolean algebra and switching functions; minterm and maxterm canonical forms; sum of products and products of sums; don't care conditions; minimization of Boolean algebra.

Combinational Logic Circuit Design
Minimization by Karnaugh map and Quine-McCluskey method; circuit designs; timing parameters and circuit hazards.

Circuit Design with Functional Blocks
Carry Look Ahead adder; comparators; decoders and encoders; multiplexers and demultiplexers.

Introduction to Hardware Description Language (HDL)
Introduction to Hardware Description Language (HDL); logic gates and combinational circuit modelling.

Flip-flops
Latches, RS, JK, D-type, edge-triggered and master-slave flip-flops; triggering and setting; timing parameters; HDL circuit modelling.

Synchronous Sequential Logic Circuit Design
Concept of states; Mealy and Moore Machines; redundant state elimination; sequential digital system analysis and design; HDL sequential circuit modelling.

Registers and Counter
Basic registers and counters; ripple counters and synchronous counters, and their applications; construction of registers and counters; HDL circuit modelling.

Field-Programmable Gate Array
Introduction to Look-up Table (LUT), Generic Array Logic (GAL), Programmable Array logic (PAL), simple programmable logic device, complex programmable logic device (CPLD), Field-Programmable Gate Array (FPGA), Programmable System-on-Chip (SoC).

FPGA Implementation
Combination and synchronous sequential circuit synthesis; datapath component description, debugging and validation.

Logic Families
Introduction to electrical characteristics of TTL and CMOS logic families; transfer characteristics, noise margins; fan-in and fan-out; comparison of families; interfacing between different families.

2. Reading List

2.1 Compulsory Readings

(Compulsory readings can include books, book chapters, or journal/magazine articles. There are also collections of e-books, e-journals available from the CityU Library.)

1.	Nil

2.2 Additional Readings

(Additional references for students to learn to expand their knowledge about the subject.)

1.	Alan B. Marcovitz: Introduction to Logic Design, Third Edition, ISBN 978-0-07-016490-1 (McGraw-Hill Higher Education 2010).
2.	Charles H Roth, Lizy K. John: Digital Systems Design Using VHDL, Fifth Edition, ISBN 978-1-305-63514-2 (Cengage Learning 2016).
3.	C V S Rao: Switching Theory & Logic Design, ISBN 81-317-0183-2 (Pearson Education 2006).
4.	Victor P. Nelson, H. Troy Nagle, Bill D. Carrol, J. David Irwin: Digital Logic Circuit Analysis and Design, ISBN 0-13-463894-8 (Prentice Hall, International Edition 1995).
5.	William J. Dally: Digital design using VHDL: a systems approach, ISBN 978-1107098862, (Cambridge University Press, 2016).