Department of Advanced Design and Systems Engineering
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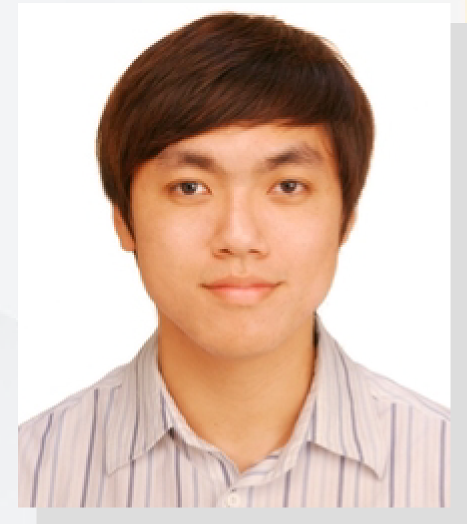
Heterogeneous integration of ultrahigh-κ perovskite membranes for two-dimensional electronics



16 Sep 2022 (Fri) | 2:30 pm

Seminar Link: https://cityu.zoom.us/j/91333634990

Dr. Jing-Kai HUANG
Lecturer/Research Associate
School of Material Science and Engineering
University of New South Wales, Australia

Abstract

For the sub-10 nm technology nodes in Si field-effect transistors (FETs), a sub-nanometer capacitance equivalent thickness (CET), and a flawless interface with the channel are essential for gate dielectrics to maintain the gate controllability. Similarly, the development of reliable high-κ dielectrics (CET < 1 nm) adaptable to 2D FETs for future nodes is eagerly awaited. The typically used high-κ dielectrics in silicon technology (i.e., SiO_2, Al_2O_3, and HfO_2) have been integrated with 2D transition metal dichalcogenide (TMD) materials. Nevertheless, their amorphous nature and imperfect dielectric/TMD interfaces make the elimination of charge scatters/traps difficult, not to mention the direct damage to 2D channels caused by dielectric deposition processes.

Here we explore transferrable ultrahigh-κ single-crystalline perovskite strontium-titanium-oxide membranes as a gate dielectric for 2D field-effect transistors. Perovskite gating exhibits a desirable sub-1 nm CET with a low leakage current (less than 10^{-2} A/cm^2 at 2.5 MV/cm). We find that the van der Waals gap between strontium-titanium-oxide dielectrics and 2D semiconductors mitigates the unfavorable fringing-induced barrier-lowering effect resulting from the use of very high-κ dielectrics. Typical short-channel transistors made of scalable molybdenum-disulfide films by chemical vapor deposition and strontium-titanium-oxide dielectrics exhibit steep subthreshold swings down to about 70 mV/dec and on/off current ratios up to 10^7, which matches the low-power specifications suggested by the latest International Roadmap for Devices and Systems (IRDS)

Reference:

J.-K. Huang*, et al., "High-κ perovskite membranes as insulators for two-dimensional transistors" **Nature** 605, 262-267 (2022).
J.-K. Huang, et al., "Crystalline Complex Oxide Membrane: Sub-1 nm CET Dielectrics for 2D Transistors" **IEEE International Electron Devices Meeting (IEDM)**, invited (2022).

About the Speaker

Dr. Jing-Kai Huang currently serves as a lecturer at the University of New South Wales (UNSW), Australia. He studied for a PhD in Material Science & Engineering from UNSW. Before receiving his PhD degree, he performed R&D works in the semiconductor at KAUST (Saudi Arabia), TSMC, and National Nano Device Laboratories (Taiwan). He has plenty of experience in nanofabrication of ultra-scaled electronic devices and strong research expertise in the scalable manufacture of 2D material thin films. Now, he focuses on the heterogeneous integration of 2D semiconductors, complex oxides (high-κ), and metal-organic frameworks (low-κ) toward the fabrication of future technology nodes.

Enquiry: 3442 8422 | All are welcome