

Semiconductor applications of plasma immersion ion implantation

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Abstract

Plasma immersion ion implantation (PIII) is an established technique in certain niche microelectronics applications such as the synthesis of silicon-on-insulator. In other applications such as shallow junction formation by plasma doping, trench doping, and fabrication of blue light emitting materials, PIII has unique advantages over conventional techniques and may be the technique of choice in the future. There have been significant developments in these areas and recent breakthroughs in plasma and trench doping are discussed in this review paper. Results pertaining to direct-current PIII that excels in planar sample processing as well as the optical characteristics of nano-cavities produced by hydrogen PIII are also presented.

1. Introduction

Plasma immersion ion implantation (PIII) was first proposed about 15 years ago to circumvent the line-of-sight restriction of conventional beam-line ion implantation [1, 2]. PIII also offers other advantages such as high throughput, large area processing, and small instrument footprint. In addition to metallurgical and tribological engineering, engineers and scientists in semiconductor and microelectronics processing have found the technology suitable [3, 4]. The most widely studied semiconductor applications of PIII are shallow junction formation by plasma doping (PD) [5–18], synthesis of silicon-on-insulator (SOI) substrates by either PIII/ion-cut or separation by plasma implantation of oxygen (SPIMOX) [19–29], conformal trench doping [30], hydrogenation of polysilicon thin films used in flat-panel displays [31], as well as fabrication of thin oxide on SiGe, low dielectric constant (low-k), and III-nitride materials [32–34]. In this review paper, recent developments in three of the areas that have seen significant development, PD, SOI formation using direct-current (DC-PIII), and fabrication of blue light emitting nano-cavities using hydrogen PIII are discussed.

2. Plasma doping

PIII is a promising doping technique for ultra-large-scale integration (ULSI) circuits. Miniaturization of silicon microelectronic devices requires ultra-shallow source/drain (S/D) extension to reduce short-channel effects and enhance the performance of the device. Shallow junctions can be accomplished using low energy in conventional beam-line ion implantation and rapid thermal annealing making use of the low thermal budget. Unfortunately, a conventional beam-line ion implantation encounters problems such as small throughput and poor beam performance as a low-energy tool [35, 36]. Moreover, three-dimensional structures with large aspect ratios are difficult to dope using conventional ion implantation, and PIII, also called PD, has attracted much attention. As an ultra-shallow junction fabrication technique, PIII (PD) has been demonstrated for both n-type and p-type ultra-shallow junctions. In order to improve the process, much work is being conducted on related issues such as high activation efficiency, reduction of damage, improvement of dopant profile steepness, and enhancement of transistor performances.

Figure 1 depicts typical applications of PIII to ULSI silicon processing [35]. Examples shown here include trench sidewall doping of deep trench-based and stack capacitor-based dynamic random access memory (DRAM), gate oxide processing, and polysilicon gate doping. A deep trench capacitor used as charge storage elements in DRAM consists of a thin insulating node film and capacitor electrodes, and the n-type region in the p-type Si substrate surrounding the trenches is the buried-plate electrode. In spite of miniaturization, the charge storage capacity of the DRAM capacitors should be maintained. In addition, as the node dielectric thickness diminishes, the n-type dopant concentration on the electrodes must be increased to mitigate the depletion capacitance. PIII as a conformal trench sidewall doping technique is thus very attractive and the process has recently been demonstrated in a deep trench with an aspect ratio of 35 : 1 [35]. Figure 2 shows a SEM micrograph of an array in a DRAM cell consisting of 6 μm deep and 0.175 μm wide trenches. The PIII process is conducted using AsH_3 plasma with a density of 10^{10} cm^{-3} . The DRAM cells are biased at 1 or 7 kV and the implant doses range from 1×10^{16} to $6 \times 10^{16} \text{ atoms cm}^{-2}$.

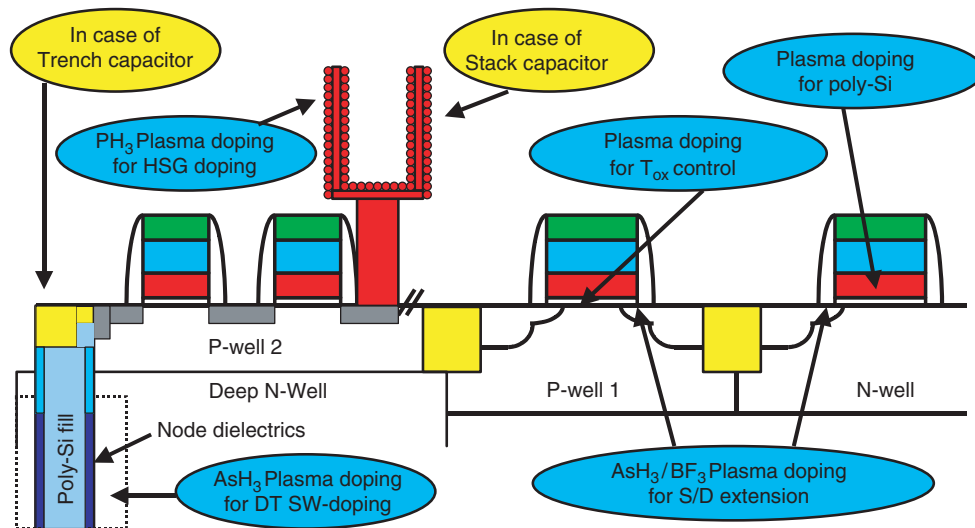


Figure 1. Application examples of PIII to ULSI silicon processing [35].

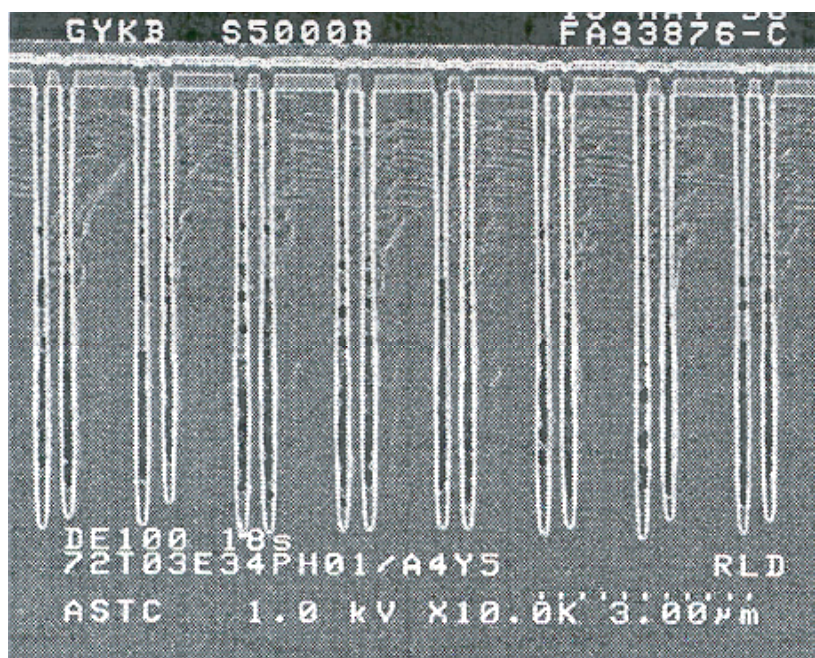


Figure 2. SEM micrograph of deep trench array in a DRAM cell [35].

3. Hydrogen PIII for SOI synthesis and DC-PIII

The use of hydrogen and helium PIII for making SOI is currently a commercial manufacturing process [37, 38] and it has been extended to perform layer transfer in other materials [39, 40]. The process requires high dose hydrogen or helium ion implantation to create micro-cavities along the projected range of the implant. Upon annealing, the stress imposed by the expansion and coalescence of these micro-cavities causes delamination of the wafer along the projected range of the implanted ions. In the silicon ion-cut process, the implanted or donor wafer is bonded to another silicon or acceptor wafer before annealing and the cleaved silicon film is transferred to the acceptor film. If the acceptor film has a surface oxide layer, the resulting structure becomes a SOI. As the required hydrogen dose for the layer transfer process is quite high, typically in the mid 10^{16} atoms cm^{-2} , PIII is a more economical alternative than conventional beam-line ion implantation. In addition to innovations in hardware, the success of PIII stems from intensive research and development on the uniformity of ion dose and implant energy as well as on other concomitant processing issues such as contamination [41–43].

In the ion-cut process, the important parameter is the depth of the hydrogen implant whereas the absolute dose is not as critical, provided that a minimal critical dose has been implanted. Hydrogen PIII is typically performed in milliTorr (0.13 Pa) or sub-milliTorr pressure to ensure non-collisional conditions in which the ion mean free path is much larger than the ion-matrix sheath thickness. However, low energy ions implanted during the rise and fall times of the voltage pulses can introduce defects affecting the yield of the ion-cut process [44–46]. There are several considerations of using negative voltage pulses in semiconductor PIII applications. When a negative high voltage pulse is imposed, the vacuum chamber, sheath, and electrical circuit inherently induce an equivalent capacitive load on the modulator inevitably giving rise to a displacement current [47]. That is, a displacement current occurs due

to the changing voltage, sheath capacitance, and circuit loads. The additional displacement currents generate extra heating to the wafer and sample stage. Deleterious metal impurities can diffuse from the contact interface and sample stage into the wafer, and are subsequently driven into the wafer at higher temperature. Therefore, cooling is sometimes required during the implantation process. During the short but finite rise and fall times of each voltage pulse, the ion acceleration energy is reduced, resulting in a low energy component in the implant distribution. Both of these effects are disadvantages in the ion cut and PIII-SIMOX techniques [48]. Hence, in order to reduce the effects of the voltage pulse rise and fall times, DC-PIII has been introduced [49–52].

Figure 3 displays a typical DC-PIII set-up employing a radio frequency (RF) plasma source. A conducting grid, made of a compatible material to avoid contamination (e.g. a silicon coated mesh for implanting silicon wafers), divides the chamber into two parts. In the lower part, a strong electric field is formed between the negatively biased wafer stage and the boundaries created by the grid and the lower part of the chamber walls. The upper part confines the plasma since the grounded grid stops the expansion of the ion sheath from the bottom. In this way, a continuous low-pressure discharge can be maintained in the volume above the grid. Positive ions diffuse into the lower part through the grid and are implanted into the wafer.

Particle-in-cell (PIC) simulation shows that the ion paths will not change with the negative voltage applied to the wafer stage, mass, and charged states of the ions, provided that their initial velocity is small compared to the electric field strength [49]. The ion path of O^+ particles at $H = 70$ cm and $H = 30$ cm are depicted in figures 4(a) and (b) for an applied voltage of -70 kV. Figure 4(a) reveals that some of the particles will pass through the mid-plane and get

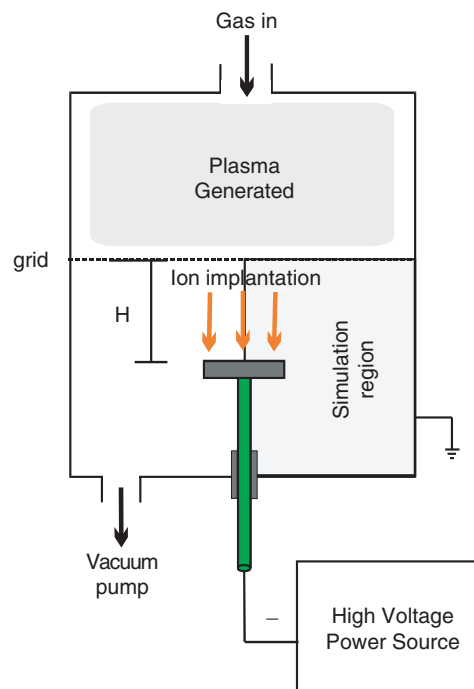


Figure 3. Schematic diagram of the steady state DC set-up for plasma implantation of semiconductor wafers. A grounded conducting grid is positioned above the wafer in the vacuum chamber.

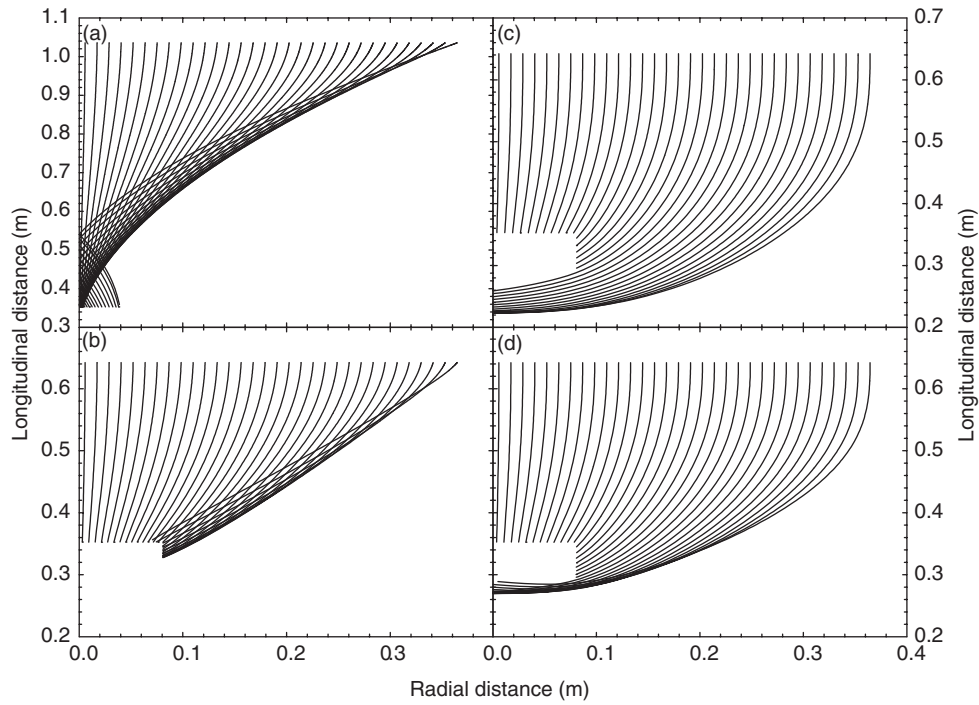


Figure 4. Simulated ion paths of the oxygen ions implanting from the grid to the wafer stage at -70 kV bias voltage: (a) The distance between the grid and wafer stage surface $H = 70$ cm showing that the ions focus onto the centre of the wafer. (b) $H = 30$ cm showing that the whole wafer is implanted. (c) An initial downward drift velocity equivalent to 5×10^3 eV energy is applied to the ions and the ion trajectories are changed. (d) O^{2+} ions with the same downward drift velocity as (c) are used in the simulation and the ion paths become dependent on the charge state at the high initial velocity of the ions.

implanted at the other half of the wafer stage. At $H = 70$ cm, the ions will focus onto the centre of the wafer stage. The ion path is determined by the velocity vector that in turn changes with the acceleration vector created by the force field in space. In addition, the directional angle does not depend on the charge state and mass of the ions. Hence, by varying the charge state of the ion and applied voltage, the impact energy can be altered, and by varying the ion mass, the final velocity of the ion will be changed. However, if the ions have a large initial drift velocity compared to the maximum velocity created by the applied voltage, they will pass through a different local field structure. In this situation, the ion paths will vary with the charge state, ion mass, and applied voltage. The ion path of the O^+ and O^{2+} particles with initial downward drift velocity $2.45 \times 10^5 \text{ m s}^{-1}$ (equal to 5 keV impact energy of oxygen ions) are displayed in figures 4(c) and (d) for $H = 30$ cm and applied voltage = -70 kV. Part of the ions have passed through the wafer stage and are implanted into the supporting rod.

The dose and energy uniformity along the implanted wafer are important issues for PIII in semiconductor applications. As mentioned before, in PIII, there is a large number of low impact energy ions introduced into the wafer during the rise and fall times of each negative voltage pulses [48]. On the other hand, in the DC mode, the ion impact energy is constant since the ions are accelerated directly from the grid to the wafer stage. The uniformity of the ion dose on the wafer depends on two factors: the uniformity of the incident ion current and impact angle. Previous studies [53] have shown that the PIII ion dose is higher at the edge of the wafer

stage when the impact angle is off normal up to 45° . Therefore, although the depth profile is shallower at the edge, the ion dose is higher. In the DC mode, the implantation area is totally determined by the ratio of the radius of wafer stage r , the radius of the vacuum chamber R , the distance between the wafer stage and grid H , and thickness of the wafer stage D . The projected area from the grid to the wafer stage determines the incident dose into the wafer. Actually, the smaller H is, the closer is the ratio of the projected area to the implanted area to 1 and the better is the incident dose uniformity. However, the shorter the distance between the anode (grid) and cathode (wafer stage), the higher is the electric field that may lead to breakdown at high implantation voltage. The impact angle at the edge can be made normal by changing the thickness of the wafer stage. A thicker wafer stage can smooth out the electric field at the edge. In PIII, the ions are accelerated from the ion sheath and the impact angle is determined by the spherical shape of the ion sheath. Hence, the retained dose and the impact energy in the DC mode can be made much more uniform by choosing the suitable internal dimensions of the lower part. It should be noted that the space charge effects of ions are not taken into account in the PIC simulation.

As aforementioned, PIII experiments are usually conducted at very low gas pressure to achieve high impact energy, for example, lower than 0.1 mTorr. Hence, a higher intensity plasma source is necessary for higher ion dose DC-PIII, e.g. electron cyclotron resonance (ECR) plasma source. Such an apparatus is shown in figure 5. To determine the ion energy distribution and dose uniformity in DC-PIII, Rutherford backscattering spectrometry (RBS) analysis was done for a 75 mm diameter silicon wafer implanted by argon DC-PIII at 30 kV. Figures 6 and 7 depict the results acquired from the centre and side of the silicon wafer, respectively. The corresponding argon depth profiles are shown in figure 8. The data agree well with the simulation result of TRIM [54] (projected range is 36.6 nm and longitudinal straggle is 14.6 nm), thereby proving that the ion impact energy is in good agreement with the DC voltage.

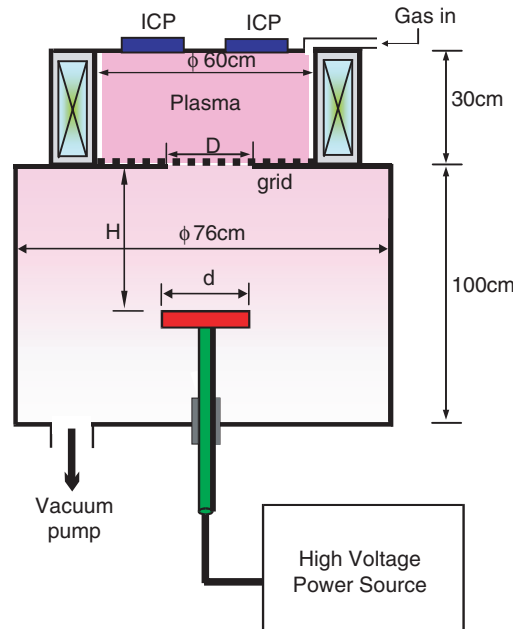


Figure 5. Schematic diagram of DC-PIII with an ECR source.

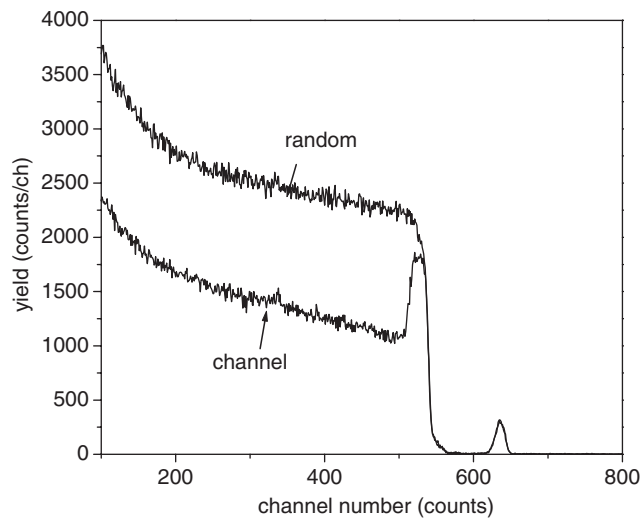


Figure 6. RBS results acquired from the centre of the 75 mm silicon wafer treated by argon DC-PIII.

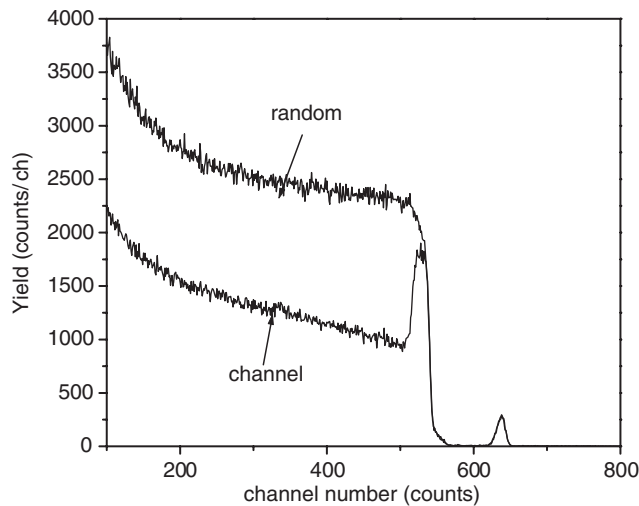


Figure 7. RBS results acquired from the edge of the 75 mm silicon wafer treated by argon DC-PIII.

The argon depth profile reveals that the ion energy is mono-energetic. The calculated doses at the centre and side of the 75 mm wafer are $3.0 \times 10^{16} \text{ cm}^{-2}$ and $2.5 \times 10^{16} \text{ cm}^{-2}$, respectively. The dose uniformity can be improved by using a more uniform plasma source and better chamber geometry. The results unequivocally indicate that the dose rate and the electrical power efficacy are significantly improved by DC-PIII. For instance, the dose rate can be as high as $1 \times 10^{17} \text{ cm}^{-2} \text{ min}^{-1}$, and the electrical power can be decreased to about one quarter of that in conventional pulse-mode PIII.

To enhance the efficacy of the DC-PIII process, the grid separating the vacuum chamber is biased. The process alters the plasma density in the plasma producing chamber and modifies the plasma topography along the grid surface. Our recent results show an enhanced extracted ion

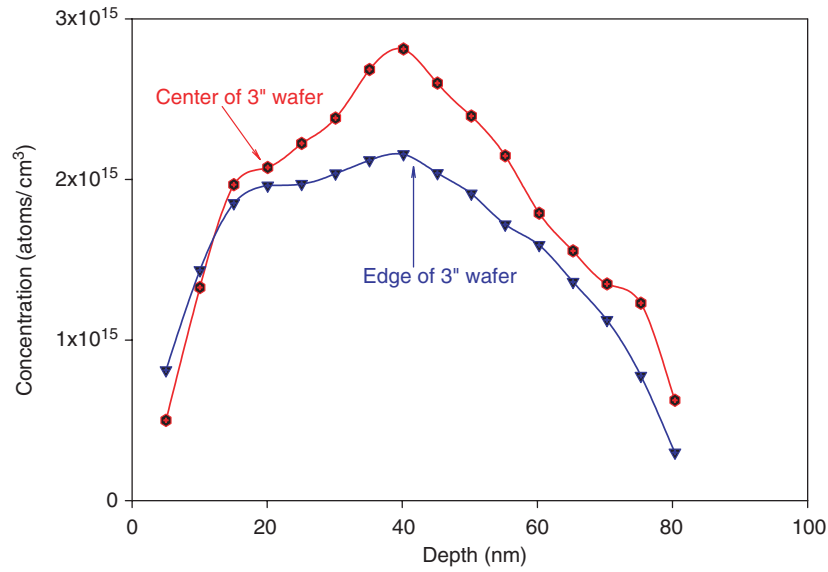


Figure 8. Argon depth profiles of the centre and the edge of the 75 mm silicon wafer treated by argon DC-PIII derived from RBS.

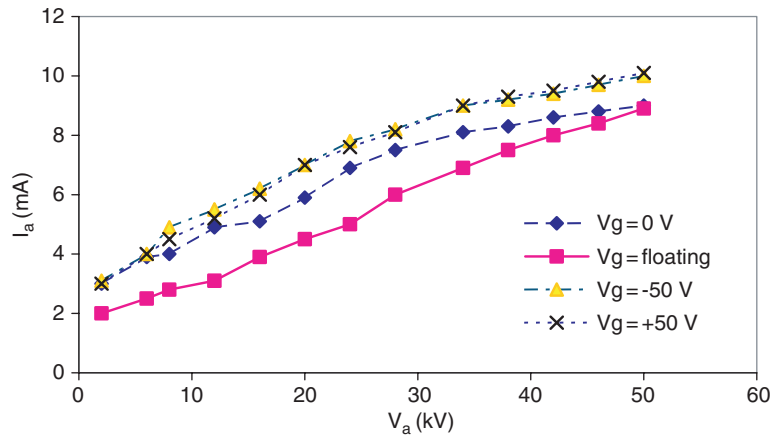


Figure 9. I_a – V_a curves for argon RF-ICP DC-PIII for grid bias voltage of 0 V, floating, –50 V, and +50 V (argon working pressure = 0.2 mTorr and RF power = 600 W).

current density from the plasma and suggest specific optimal process windows [55]. Figure 9 plots the measured current at the wafer stage (I_a) for different grid bias (V_g) as a function of the applied DC voltages (V_a) at an RF power of 600 W. The data were acquired in an RF-ICP plasma at a low pressure of 0.2 mTorr. No glow discharge was observed in the vicinity of the wafer stage throughout the experiment, and the smooth I_a – V_a relationship in figure 9 supports the visual observation. This is due to the relatively large argon ion-neutral mean free path (about 20 cm) beneath the grid. The current V_a increases monotonically with the grid voltage V_g in all four cases. Based on our PIC simulation results, all ions extracted through the holes on the grid bombard the wafer stage without loss and so it is reasonable to think that the I_a – V_a relationship

only depends on the secondary electron emission coefficient γ , i.e. $I_a = (1 + \gamma)I_i$ where I_i is the ion current. In the experiment, the calculated value of $[1 + \gamma(40 \text{ kV})]/[1 + \gamma(30 \text{ kV})]$ is in the range of 1.08–1.15 and agrees well with Shamim's value of 1.02 [56]. The slope of the curve is steeper at low V_a due to a bigger variation of γ with V_a .

Figures 10 and 11 display the relationship of I_a versus the argon pressure and RF power at a sample voltage of -20 kV for $V_g = 0 \text{ V}$ and $+50 \text{ V}$. The $+50 \text{ V}$ grid voltage appears to be the optimal value with respect to glow discharge between the grid and the chamber. It can be readily observed that I_a increases with argon pressure and RF power. Our PIC simulation results exhibited in figure 12 indicate that all extracted ions bombard the wafer within a diameter of about 110 mm . This is consistent with our observation during the experiment that light converges onto the central area of the wafer stage. The simulation data illustrate that the implantation area is almost the same for all biasing voltages at $V_a = -20 \text{ kV}$. Thus, the implantation current density can be represented by I_a in all these cases. Figure 13 shows the relationship of I_a with V_g at $V_a = -20 \text{ kV}$. I_a drops precipitously as the voltage increases from zero to positive and achieves a minimum value at a grid voltage of about $+10.5 \text{ V}$, followed by a gradual increase saturating at about $+50 \text{ V}$. For a negative bias, the current slowly increases as the voltage decreases, and the current reaches saturation slightly below -50 V . It is also

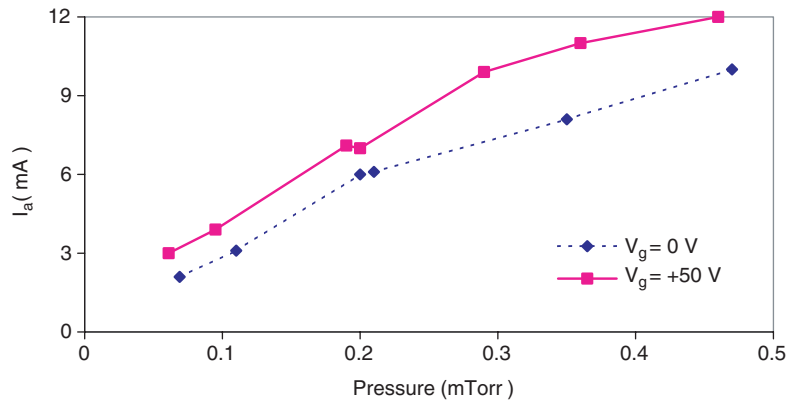


Figure 10. I_a versus argon pressure at $V_a = -20 \text{ kV}$ for $V_g = 0, +50 \text{ V}$ (RF power = 600 W).

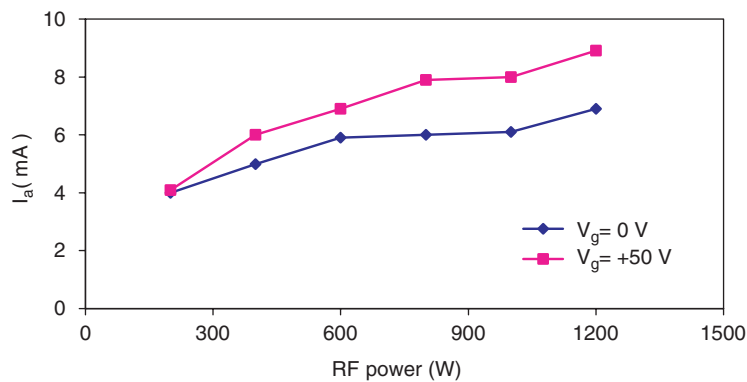


Figure 11. I_a versus RF power at $V_a = -20 \text{ kV}$ for $V_g = 0, +50 \text{ V}$ (argon pressure = 0.2 mTorr).

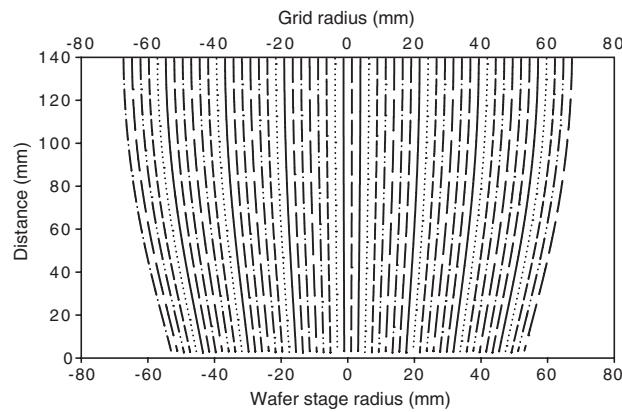


Figure 12. Simulated trajectories of argon ions from the grid impinging into the wafer stage at $V_a = -20$ kV and $V_g = 0$ V. The distance between the grid and wafer stage is 140 mm and the diameter of the grid and wafer stage is 150 mm.

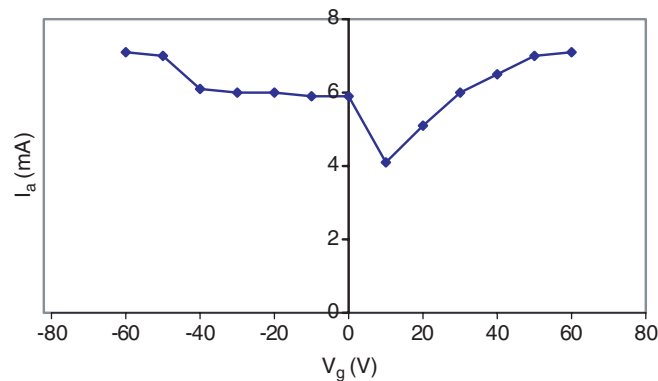


Figure 13. Relationship of I_a with the grid bias at $V_a = -20$ kV (argon pressure = 0.2 mTorr and RF power = 600 W).

Table 1. Retained argon dose measured by RBS from the centre of silicon wafers implanted using different V_g (pressure = 0.2 mTorr, RF = 600 W, $V_a = -20$ kV, and implantation time = 8 min).

V_g	0 V	Floating	-50 V	+50 V
Retained dose ($\times 10^{16}$ cm $^{-2}$)	1.8	1.2	2.6	2.6

observed that the minimum I_a is equal to that when the potential floats, that is, with the grid not grounded nor biased, and so the floating potential is +10.5 V.

Table 1 shows the retained argon doses measuring by RBS from the centre of silicon wafers implanted at $V_a = -20$ kV for $V_g = 0$ V, floating, -50 V, and +50 V. The total implantation time was 8 min and the pressure was 0.2 mTorr. The increase in the implantation dose with a grid bias compared to that when using a grounded or floating grid is obvious, even though there is no clear improvement in the lateral uniformity of the implant dose on the 150 mm silicon wafer using grid biasing. The lateral uniformity can be more easily addressed by improving the uniformity of the plasma, for instance, using a better RF-ICP hardware design. Similar experiments were performed using a hydrogen plasma and the results show that the I_a - V_g curve

for hydrogen is similar, even though the discharge characteristics should be more complicated in hydrogen plasma due to the presence of multiple ion species. Our results thus show that grid biasing is a useful means to improve the implantation efficiency of hydrogen DC-PIII in the ion-cut process.

4. Blue light emission from nano-cavities produced by hydrogen PIII

There is a commercial need for an optical emitter that is compatible with standard, silicon-based ULSI technology. Applications where silicon-based light emitters can be utilized include data transceivers for local area networks, optical interconnects for high speed system integration, and low-cost, high-resolution displays. Bulk silicon, unfortunately, can only emit weak infrared light at cryogenic temperature because of its narrow and indirect band gap. In order to obtain visible light, there is much interest to modify the bandgap of silicon, a process termed 'bandgap engineering'. The common objective is to increase the bandgap of silicon or to introduce radiative centres.

Nano-cavities formed after hydrogen PIII implantation create internal stress and layer transfer can be accomplished if the implanted wafer is bonded to an acceptor wafer. Optically, these buried nano-cavities exhibit photoluminescence (PL) characteristics like porous silicon but because they are protected by a surface silicon layer, the 'buried porous silicon' structure is more stable than porous silicon fabricated by conventional anodization [29]. These nano-cavities are separated by an average distance on the same order of the size of the confinement action in porous silicon [57].

Figure 14 depicts the 10.7 K low temperature PL spectra acquired from hydrogen plasma implanted silicon samples (10^{17} cm^{-2} dose and 10 kV implantation voltage) samples annealed at different temperatures. A peak at 888 nm is observed from samples annealed at 200°C and 400°C, and the intensities increase with temperature in this range. However, PL cannot be observed from the sample annealed at 600°C. The PL spectra as a function of measurement temperature were also acquired. The PL intensities decrease with increasing measurement temperature, and are very weak at room temperature. On the other hand, the electroluminescence (EL) results are quite different from those of PL. EL is observed only from samples annealed at temperature higher than 600°C. Figure 15 shows the EL spectra from the sample annealed at 600°C under different applied voltages. The EL intensities increase with

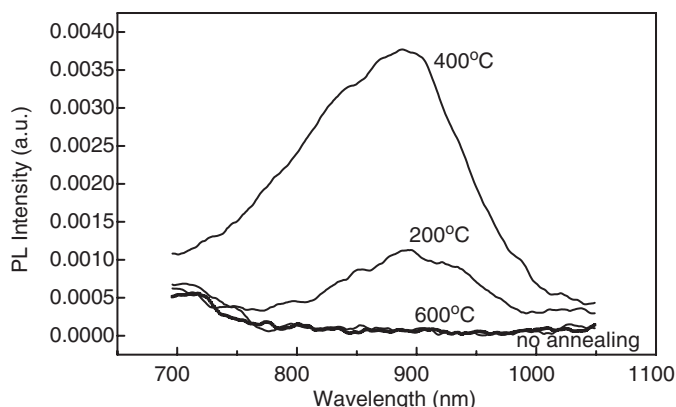


Figure 14. PL spectra acquired cryogenically at 10.7 K from hydrogen plasma-implanted silicon annealed at different temperature. The excitation wavelength is 325 nm.

higher applied voltages and a ‘blue shift’ is observed with increasing voltage. Unlike the PL intensities, the EL signals at room temperature are intense enough for the naked eyes. The EL emission is white and quite broad, from 400 to 800 nm, and the main peak is at 578 nm.

The different PL and EL characteristics suggest that their mechanisms are different. The luminescence properties depend greatly on the annealing temperature after hydrogen implantation. In the FTIR spectra exhibited in figure 16, peaks at 454 cm^{-1} , 627 cm^{-1} , and $1040\text{--}1160\text{ cm}^{-1}$ represent Si–O–Si bending, Si–H₂ deformation, and Si–O–Si stretching, respectively. No other silicon and hydrogen bonds can be detected. The intensity of the Si–H₂ deformation peak does not change until the annealing temperature reaches 600°C . Hence, it appears that hydrogen combines with silicon to form SiH₂ when the temperature is below 600°C . However, when the temperature reaches 600°C , hydrogen begins to diffuse out of the

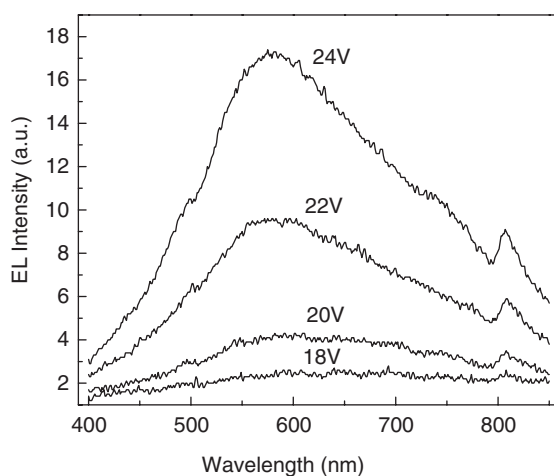


Figure 15. EL spectra acquired at room temperature from hydrogen plasma-implanted silicon annealed at 600°C . The applied voltage varies from 18 to 24 V.

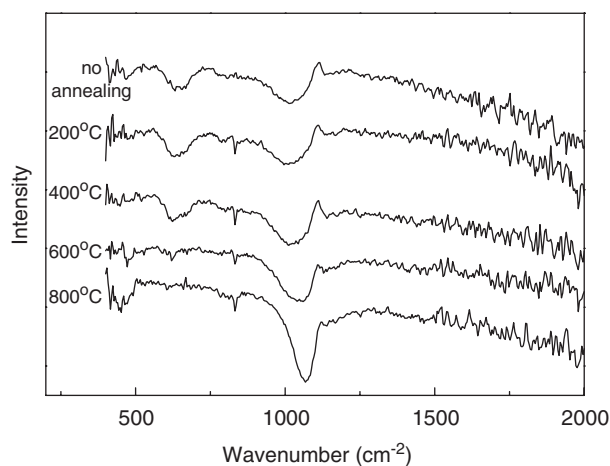


Figure 16. FTIR spectra obtained from hydrogen plasma implanted silicon annealed at different temperature.

sample, a phenomenon confirmed by secondary ion mass spectrometry (SIMS) profiling (not shown here).

The microstructures of the hydrogen-implanted silicon are investigated by TEM. Owing to the absence of mass analysis in PIII, three hydrogen species, namely H^+ , H_2^+ , and H_3^+ , are implanted simultaneously but their net implantation energies are different (for instance, each H in the H_3^+ molecular ion has $\frac{1}{3}$ the energy). Therefore, there is a broader defect region in the plasma-implanted silicon sample. In spite of the high implant dose, no surface blisters (local exfoliation) can be found on the sample annealed at 400°C, as shown in figure 17(a). However, the TEM micrograph acquired from the sample annealed at 600°C displayed in figure 17(b) is quite different. The defect zone still exists, but buried cavities several hundred nanometers in

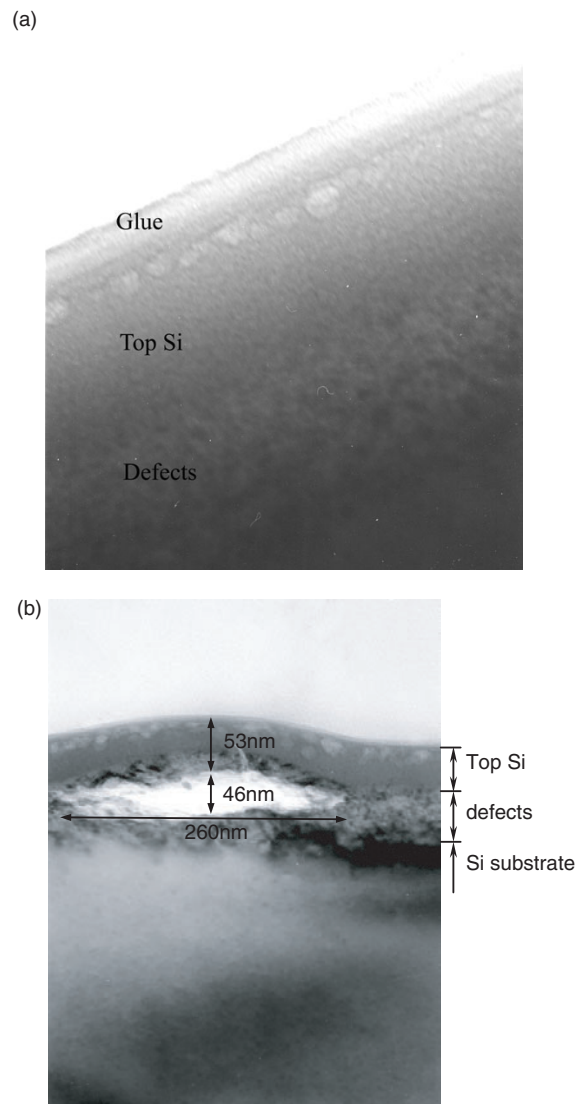


Figure 17. Cross-sectional TEM micrographs of the hydrogen plasma-implanted silicon annealed at (a) 400°C and (b) 600°C.

size can be observed. Surface ripples resembling arches can also be seen and they are due to the pressure exerted by the underlying nano-cavities.

Two mechanisms can be postulated: (a) quantum confinement effects in Si nanocrystals produced by hydrogen implantation and (b) hydrogen inhibition of nonradiative recombination centres. Our results show that the PL intensities depend greatly on the measurement temperature. Therefore, non-radiative centres appear to play an important role since the band-to-band transition is relatively temperature independent. The TEM results show many dislocation loops in the hydrogen-implanted silicon and the PL properties are probably related to both the presence of hydrogen and these dislocations. The proposed PL mechanism, however, cannot explain the EL phenomenon. When the annealing temperature reaches 600°C, the hydrogen content is reduced due to out-diffusion but strong EL emerges. Hence, hydrogen is not a key to EL and it also does not appear that the main mechanism is quantum confinement in the nano-cavities or dislocation loops since dislocation loops are also observed in samples annealed between 400°C and 600°C. Since the biggest difference among these samples is the surface topography, the surface structures formed at 600°C may be responsible for the EL behaviour. The stress around the structures is quite high as shown by the surface undulation exhibited in figure 17(b). In this sample, the buried cavities form at 50 nm below the surface and the average distance between them is 10 μm . Similar characteristics are observed from another sample plasma implanted at 25 kV, and 600°C appears to be the threshold as no EL is observed from samples annealed at a lower temperature. Subsequent work discloses that the EL intensities increase with higher nano-cavity density. It appears that the strain caused by these surface structures modifies the bandgap of the materials and more experiments are being conducted to elucidate the relationship and mechanism in more details.

5. Conclusion

PIII has found a number of exciting applications in semiconductors and microelectronics. PD is gaining momentum to replace conventional beam-line ion implantation in trench doping and shallow junction formation. Hydrogen PIII as practiced in the layer transfer technology has gained a lot of ground in terms of ion dose/energy uniformity and contamination, and rivals beam-line ion implantation as a commercial technique. The advent of DC-PIII obviates the need of the complicated and expensive power modulator and significantly reduces the instrument footprint. This novel technique may find its way into commercial SOI fabrication and other semiconductor processes. Blue light emission from hydrogen plasma implanted silicon offers an exciting way of integrating microelectronic and optical devices on the same silicon wafer.

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