SYE6206: PACKAGING FOR NANOELECTRONICS

Effective Term
Semester A 2025/26

Part I Course Overview

Course Title
Packaging for Nanoelectronics

Subject Code
SYE - Systems Engineering
Course Number
6206

Academic Unit
Systems Engineering (SYE)

College/School
College of Engineering (EG)

Course Duration
One Semester

Credit Units
3

Level
P5, P6 - Postgraduate Degree

Medium of Instruction
English

Medium of Assessment
English

Prerequisites
Nil

Precursors
Nil

Equivalent Courses
ADSE6206 Packaging for Nanoelectronics (offered until 2023/24)

Exclusive Courses
Nil

Part II Course Details

Abstract
Packaging for Nanoelectronics is an advanced course that focuses on specialized packaging technologies for nanoelectronic devices. It covers the challenges, requirements, and advancements in nanoscale packaging, including system integration,

interconnects, and management. The course explores various topics such as design considerations, advanced materials, and interconnect technologies. It also delves into the reliability aspects of nanoelectronic packaging, addressing concerns such as electromigration, thermal cycling, and mechanical stress. Real-world case studies and examples are incorporated to provide practical insights and enhance understanding. The course highlights emerging trends and future directions in nanoelectronics packaging. By the end of the course, students will possess the skills necessary to design, analyze, and optimize packaging solutions for nanoelectronic devices, considering the unique challenges and requirements at the nanoscale.

Course Intended Learning Outcomes (CILOs)

	CILOs	Weighting (if app.)	DEC-A1	DEC-A2	DEC-A3
1	Understand the fundamental principles and challenges associated with packaging for nanoelectronics, including the impact of nanoscale devices on packaging requirements and limitations.	25	x	x	
2	Develop proficiency in designing and optimizing packaging solutions for nanoelectronic devices.	25	x	x	
3	Analyze and evaluate the reliability aspects of nanoelectronic packaging, including the identification and mitigation of failure mechanisms.	25	x	x	
4	Apply advanced packaging materials and interconnect technologies suitable for nanoscale devices, including nanowires, nanotubes, and 2D materials, to ensure reliable and efficient operation of nanoelectronic systems.	25	x	x	

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to real-life problems.

A3: Accomplishments
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

Learning and Teaching Activities (LTAs)

	LTAs	Brief Description	CILO No.	Hours/week (if applicable)
1	Lecture	Lectures on the topics of the keyword syllabus.	1, 2, 3, 4	3 hours/week
2	Mini project	Team-based mini project	1, 2, 3, 4	3 hours/semester

Assessment Tasks / Activities (ATs)

	ATs	CILO No.	Weighting (%)	Remarks ("-" for nil entry)	Allow Use of GenAI?
1	Mid-term exam	1, 2, 3, 4	30	-	No
2	Mini project report	1, 2, 3, 4	20	-	No

Continuous Assessment (%)

50

Examination (%)

50

Examination Duration (Hours)

2

Minimum Continuous Assessment Passing Requirement (%)

30

Minimum Examination Passing Requirement (%)

30

Assessment Rubrics (AR)

Assessment Task

Mid-term exam (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion

Understand nanoelectronics packaging principles, challenges, and limitations. Develop proficiency in designing optimized solutions, considering signal integrity, power, miniaturization, and thermal management.

Excellent

(A+, A, A-) High

Good

(B+, B, B-) Significant

Fair

(C+, C, C-) Moderate

Marginal

(D) Basic

Failure

(F) Not even reaching marginal levels

Assessment Task

Mini project (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion

Apply the knowledge acquired to address practical issues through teamwork and oral presentation.

Excellent

(A+, A, A-) High

Good

(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal levels

Assessment Task
Final exam (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Understand nanoelectronics packaging principles, challenges, and limitations. Design optimized solutions considering signal integrity, power, miniaturization, thermal management. Analyze reliability aspects and apply advanced materials/ interconnects for robust nanoelectronic packages.

Excellent
(A+, A, A-) High

Good
(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal levels

Assessment Task
Mid-term exam (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Understand nanoelectronics packaging principles, challenges, and limitations. Develop proficiency in designing optimized solutions, considering signal integrity, power, miniaturization, and thermal management.

Excellent
(A+, A, A-) High

Good
(B+, B) Significant

Marginal
(B-, C+, C) Moderate/Basic

Failure
(F) Not even reaching marginal levels

Assessment Task

Mini project (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion

Apply the knowledge acquired to address practical issues through teamwork and oral presentation.

Excellent

(A+, A, A-) High

Good

(B+, B) Significant

Marginal

(B-, C+, C) Moderate/Basic

Failure

(F) Not even reaching marginal levels

Assessment Task

Final exam (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion

Understand nanoelectronics packaging principles, challenges, and limitations. Design optimized solutions considering signal integrity, power, miniaturization, thermal management. Analyze reliability aspects and apply advanced materials/ interconnects for robust nanoelectronic packages.

Excellent

(A+, A, A-) High

Good

(B+, B) Significant

Marginal

(B-, C+, C) Moderate/Basic

Failure

(F) Not even reaching marginal levels

Part III Other Information

Keyword Syllabus

- Packaging for Nanoelectronics
- Specialized technologies for nanoelectronic devices
- Challenges, requirements, and advancements in nanoscale packaging
- System integration, interconnects, and thermal management
- Design considerations, advanced materials, and interconnect technologies
- Real-world case studies and examples for practical insights
- Emerging trends and future directions in nanoelectronics packaging

Reading List

Compulsory Readings

	Title
1	"Advanced Packaging and Manufacturing Technology for Micro- and Nanoelectronics" edited by Feng Xue and S.J. Chua, published by CRC Press, 2020.

Additional Readings

	Title
1	NIL