SYE6204: VLSI/ULSI PROCESS INTEGRATION

Effective Term
Semester A 2025/26

Part I Course Overview

Course Title
VLSI/ULSI process integration

Subject Code
SYE - Systems Engineering
Course Number
6204

Academic Unit
Systems Engineering (SYE)

College/School
College of Engineering (EG)

Course Duration
One Semester

Credit Units
3

Level
P5, P6 - Postgraduate Degree

Medium of Instruction
English

Medium of Assessment
English

Prerequisites
Nil

Precursors
Nil

Equivalent Courses
ADSE6204 VLSI/ULSI process integration (offered until 2023/24)

Exclusive Courses
Nil

Part II Course Details

Abstract
The aim of this course is to provide students with a basic understanding of very large-scale integration (VLSI), the process of creating an integrated circuit (IC) by combining millions or billions of MOS transistors onto a single chip. An understanding

of modern logic design is crucial to chip manufacturing, as almost all digital systems today are based on VLSI chips. The course will provide an overview of the MOS transistors and IC fabrication and develop abstractions to create and reason about complex digital systems. This course serves as an introduction to back-end VLSI design fundamentals, as well as various computer-aided design (CAD) tools and methodologies.

Course Intended Learning Outcomes (CILOs)

	CILOs	Weighting (if app.)	DEC-A1	DEC-A2	DEC-A3
1	Understanding of MOS transistors	25	x	x	
2	Understanding of micro-fabrication processes	25	x	x	
3	Basic VLSI design	25	x	x	
4	Testing, reliability, power and performance	25	x	x	

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to real-life problems.

A3: Accomplishments
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

Learning and Teaching Activities (LTAs)

	LTAs	Brief Description	CILO No.	Hours/week (if applicable)
1	Lecture	Lectures on the topics of the keyword syllabus.	1, 2, 3, 4	3 hours/week

Assessment Tasks / Activities (ATs)

	ATs	CILO No.	Weighting (%)	Remarks ("-" for nil entry)	Allow Use of GenAI?
1	Mid-term exam	1, 2, 3, 4	30	-	No

Continuous Assessment (%)

30

Examination (%)

70

Examination Duration (Hours)

2

Minimum Continuous Assessment Passing Requirement (%)

30

Minimum Examination Passing Requirement (%)

30

Assessment Rubrics (AR)

Assessment Task
Mid-term exam (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Understand some of the techniques, skills, and modern trends for VLSI technology.

Excellent
(A+, A, A-) High

Good
(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal levels

Assessment Task
Final exam (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Apply the knowledge of mathematics, science and engineering to VLSI technology.

Excellent
(A+, A, A-) High

Good
(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal levels

Assessment Task
Mid-term exam (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Understand some of the techniques, skills, and modern trends for VLSI technology.

Excellent
(A+, A, A-) High

Good
(B+, B) Significant

Marginal
(B-, C+, C) Moderate/Basic

Failure
(F) Not even reaching marginal levels

Assessment Task
Final exam (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Apply the knowledge of mathematics, science and engineering to VLSI technology.

Excellent
(A+, A, A-) High

Good
(B+, B) Significant

Marginal
(B-, C+, C) Moderate/Basic

Failure
(F) Not even reaching marginal levels

Part III Other Information

Keyword Syllabus

- Overview of VLSI systems
- MOS transistor theory
- Layout design rules
- IC fabrication
- MEMs and Memory system
- Testing, reliability, power and performance

Reading List

Compulsory Readings

	Title
1	Fundamentals of Modern VLSI Devices, Cambridge University Press, 2013
2	VLSI Fabrication Principles: Silicon and Gallium Arsenide, Wiley, 2008
3	VLSI Technology, McGraw Hill Education, 2017

Additional Readings

	Title
1	NIL