EE6625: HARDWARE ARCHITECTURES FOR ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING

New Syllabus Proposal

Effective Term
Semester A 2026/27

Part I Course Overview

Course Title
Hardware Architectures for Artificial Intelligence and Machine Learning

Subject Code
EE - Electrical Engineering
Course Number
6625

Academic Unit
Electrical Engineering (EE)

College/School
College of Engineering (EG)

Course Duration
One Semester

Credit Units
3

Level
P5, P6 - Postgraduate Degree

Medium of Instruction
English

Medium of Assessment
English

Prerequisites
Nil

Precursors
Nil

Equivalent Courses
Nil

Exclusive Courses
Nil

Part II Course Details

Abstract

This course provides an introduction of how developments in deep learning algorithms have influenced hardware design advancements in recent time. It discusses bottlenecks of traditional computer architecture and introduces new paradigms including compute-in-memory and neuromorphic computing, as well as developments in conventional computing architectures and specialized machine learning accelerators. Also, create algorithm-hardware co-design strategies for creating and refining hardware specifically for deep learning algorithms will be developed by the students.

Course Intended Learning Outcomes (CILOs)

	CILOs	Weighting (if app.)	DEC-A1	DEC-A2	DEC-A3
1	Recognize problems related to conventional computer architecture for implementing popular AI/ML algorithms		x	x	
2	Design Digital Accelerators for popular AI/ML algorithms		x	x	x
3	Design In-memory Computing Accelerators for popular AI/ML algorithms		x	x	x
4	Apply Hardware/Software co-design to Reduce Hardware requirements of popular AI/ML algorithms.		x	x	x

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to real-life problems.

A3: Accomplishments
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

Learning and Teaching Activities (LTAs)

	LTAs	Brief Description	CILO No.	Hours/week (if applicable)
1	Lectures	Key concepts described	1, 2, 3, 4	3
2	Laboratories	Learned concepts are applied	2, 3, 4	3 (4 weeks)

Assessment Tasks / Activities (ATs)

	ATs	CILO No.	Weighting (%)	Remarks ("-" for nil entry)	Allow Use of GenAI?
1	Tests	1, 2, 3, 4	30	summative assessment tasks	No
2	Lab exercise	2, 3, 4	10	formative assessment tasks	Yes

3	Assignment	1, 2, 3, 4	10	formative assessment tasks	Yes

Continuous Assessment (%)
50

Examination (%)
50

Examination Duration (Hours)
2

Minimum Continuous Assessment Passing Requirement (%)
30

Minimum Examination Passing Requirement (%)
30

Additional Information for ATs
To pass the course, students are required to achieve at least 30% in course work and 30% in the examination.

Assessment Rubrics (AR)

Assessment Task
Examination (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good
(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal level

Assessment Task
Coursework (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good

(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal level

Assessment Task
Examination (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good
(B+, B) Medium

Marginal
(B-, C+, C) Low

Failure
(F) Not even reaching marginal level

Assessment Task
Coursework (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good
(B+, B) Medium

Marginal
(B-, C+, C) Low

Failure
(F) Not even reaching marginal level

Additional Information for AR
Constructive Alignment with Programme Outcomes
PILO 1: This course describes how computer hardware is changing to address the needs of AI applications

PILO 2: This course evaluates and analyses new computer architectures such as in-memory computing, digital hardware accelerators for AI.

PILO 3: Special knowledge of new methods of hardware accelerator design and hardware-software co-design of AI algorithms will be applied

PILO 4: Students will assess problems and solutions related to speed/latency and energy efficiency of computer hardware running modern AI algorithms

Part III Other Information

Keyword Syllabus

a. Different AI/ML algorithms
b. Need for specialized hardware – slowdown of Moore’s law, von Neumann bottleneck etc.
c. Digital accelerator techniques e.g. systolic arrays, weight stationary etc.
d. Software/hardware co-design e.g. quantization, sparsity etc.
e. Memory issues and compute -in-memory e.g. RRAM, SRAM CIM designs
f. Advanced topics e.g. neuromorphic computing by SNNs, network on chip etc.

Reading List

Compulsory Readings

	Title
1	Nil

Additional Readings

	Title
1	https://tinymlbook.com/
2	Deep Learning (Adaptive Computation and Machine Learning series) by Ian Goodfellow (Author), Yoshua Bengio (Author), Aaron Courville (Author)
3	Deep Learning for Computer Architects (Synthesis Lectures on Computer Architecture) 1st Edition by Brandon Reagen (Author), Robert Adolf (Author), Paul Whatmough (Author), Gu-Yeon Wei (Author), David Brooks (Author)
4	“Efficient Processing of Deep Neural Networks (Synthesis Lectures on Computer Architecture)”, by Vivienne Sze (Author), Yu-Hsin Chen (Author), Tien-Ju Yang (Author), Joel S. Emer (Author)