EE5430: ADVANCED CMOS TECHNOLOGY

Effective Term
Semester A 2025/26

Part I Course Overview

Course Title
Advanced CMOS Technology

Subject Code
EE - Electrical Engineering
Course Number
5430

Academic Unit
Electrical Engineering (EE)

College/School
College of Engineering (EG)

Course Duration
One Semester

Credit Units
3

Level
P5, P6 - Postgraduate Degree

Medium of Instruction
English

Medium of Assessment
English

Prerequisites
Nil

Precursors
Nil

Equivalent Courses
Nil

Exclusive Courses
Nil

Additional Information
Nil

Part II Course Details

Abstract

This course aims to provide the students with advanced CMOS technology knowledge required for VLSI circuits and system designs. Emphasis is placed on understanding the characteristics and limitations of nanoscale CMOS devices and the fabrication processes. The students will learn the device designs and process by the state-of-the-art CAD tools.

Course Intended Learning Outcomes (CILOs)

	CILOs	Weighting (if app.)	DEC-A1	DEC-A2	DEC-A3
1	Describe the processes and techniques used in nanoscale CMOS device and circuit fabrication.		x		
2	Understand the limitations and their solutions of nanoscale CMOS devices for integration.		x		
3	Derive the model equations for characterizing the short channel effects, and figures of merit of nanoscale CMOS transistors.		x		

A1: Attitude
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: Ability
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to real-life problems.

A3: Accomplishments
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

Learning and Teaching Activities (LTAs)

	LTAs	Brief Description	CILO No.	Hours/week (if applicable)
1	Lecture	Introduction to CMOS technology	1, 2, 3	
2	Laboratory	Lab sessions with hand-on experience, for the latest fabrication technology and device measurements techniques	1, 2, 3	
3	Case study	Presentation and group discussion of various technology options	1, 2, 3	

Assessment Tasks / Activities (ATs)

	ATs	CILO No.	Weighting (%)	Remarks ("-" for nil entry)	Allow Use of GenAI?
1	Assessment (> 3 times)	1, 2, 3	15	-	Yes
2	Test (2 times)	1, 2	20	-	No

3	Case study and presentation	1, 2, 3	10	-	Yes
4	Lab report	1, 2, 3	5	-	Yes

Continuous Assessment (%)
50

Examination (%)
50

Examination Duration (Hours)
2

Minimum Continuous Assessment Passing Requirement (%)
30

Minimum Examination Passing Requirement (%)
30

Additional Information for ATs
To pass the course, students are required to achieve at least 30% in course work and 30% in the examination.

Assessment Rubrics (AR)

Assessment Task
Examination (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good
(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal level

Assessment Task
Coursework (for students admitted before Semester A 2022/23 and in Semester A 2024/25 & thereafter)

Criterion
Achievements in ClLOs

Excellent
(A+, A, A-) High

Good
(B+, B, B-) Significant

Fair
(C+, C, C-) Moderate

Marginal
(D) Basic

Failure
(F) Not even reaching marginal level

Assessment Task
Examination (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good
(B+, B) Medium

Marginal
(B-, C+, C) Low

Failure
(F) Not even reaching marginal level

Assessment Task
Coursework (for students admitted from Semester A 2022/23 to Summer Term 2024)

Criterion
Achievements in CILOs

Excellent
(A+, A, A-) High

Good
(B+, B) Medium

Marginal
(B-, C+, C) Low

Failure
(F) Not even reaching marginal level

Part III Other Information

Keyword Syllabus

Syllabus discusses the topics of:

CMOS Technology and Fabrication Processes,

Nanoscale MOSFETs,

Challenges of Giga-Scale Integration.

CMOS Technology Overview: Evolution and recent advances in silicon electronics, Moore's Law and the ITRS, State-of-the-Art CMOS technology.

Overview on Nano-CMOS Fabrication Processes: Overview of basic silicon processing steps, Subwavelength photolithography, Ultra-shallow junction fabrication, atomic layer deposition technique, plasma etching, advanced interconnects technologies.

Nanoscale MOSFETs: MOSFET figures of merit: on and off current, CVI metric, gate delay, power-delay product.

Nanometer bulk MOSFETs: issues of downsizing, doping profiles, high-k dielectrics, gate stack design.

Non-classical MOSFET structures: transport enhanced MOSFETs (strained Si and SiGe, Ge), SOI MOSFETs, multiple gate MOSFETs (lateral double-gate MOSFET, FinFET, Tri-gate MOSFET).

Problems and challenges of nanoscale MOSFETs: performance degradation, the limits of scaling (physical and process constraints).

Challenges of Giga-Scale Integration: Reliability and yield, interconnets and delay, power dissipation and thermal issues, economics issues, Si optoelectronic components.

Reading List

Compulsory Readings

	Title
1	Textbooks aren't necessary. Your attendance + notes should be adequate for examination. Below is a list of commonly used references, I have only flipped through a few, though.

Additional Readings

	Title
1	F. Schwierz, H. Wong, and J. J. Liou: Nanometer CMOS, (Pan Stanford Publishing, 2010)
2	H. Wong, Nano-CMOS Gate Dielectric Engineering, (CRC Press, 2011)
3	B. Razavi, "Design of Analog CMOS Integrated Circuits", New York: McGraw Hill.
4	Analysis and Design of Elementary MOS Amplifier Stages (https://github.com/bmurmann/Book-on-MOS-stages), Copyright (c) 2013-2022 National Technology and Science Press, Copyright (c) 2022 Boris Murmann