City University of Hong Kong
Course Syllabus

offered by Department of Electrical Engineering
with effect from Semester A 2022/2023

Part I Course Overview

Course Title:	Advanced CMOS Technology
Course Code:	EE5430
Course Duration:	One Semester (13 weeks)
Credit Units:	3
Level:	P5
Medium of Instruction:	English
Medium of Assessment:	English
Prerequisites: *(Course Code and Title)*	Nil
Precursors: *(Course Code and Title)*	EE3115 Applied Optoelectronic Devices or EE3132 Microelectronic Circuit Designs
Equivalent Courses: *(Course Code and Title)*	Nil
Exclusive Courses: *(Course Code and Title)*	Nil

Part II Course Details

1. Abstract

This course aims to provide the students with advanced CMOS technology knowledge required for VLSI circuits and system designs. Emphasis is placed on understanding the characteristics and limitations of nanoscale CMOS devices and the fabrication processes. The students will also be provided with hands-on experience in device designs and process simulations using the state-of-the-art CAD tools.

2. Course Intended Learning Outcomes (CILOs)

(CILOs state what the student is expected to be able to do at the end of the course according to a given standard of performance.)

No.	CILOs	Weighting (if applicable)	Discovery-enriched curriculum related learning outcomes (please tick where appropriate)		
			A1	*A2*	*A3*
1.	Describe the processes and techniques used in nanoscale CMOS device and circuit fabrication.		✓		
2.	Understand the limitations and their solutions of nanoscale CMOS devices for gigascale integration.		✓		
3.	Derive the model equations for characterizing the short-channel effects, and figures of merit of nanoscale CMOS transistors.		✓		
		100%			

A1: *Attitude*
Develop an attitude of discovery/innovation/creativity, as demonstrated by students possessing a strong sense of curiosity, asking questions actively, challenging assumptions or engaging in inquiry together with teachers.

A2: *Ability*
Develop the ability/skill needed to discover/innovate/create, as demonstrated by students possessing critical thinking skills to assess ideas, acquiring research skills, synthesizing knowledge across disciplines or applying academic knowledge to self-life problems.

A3: *Accomplishments*
Demonstrate accomplishment of discovery/innovation/creativity through producing /constructing creative works/new artefacts, effective solutions to real-life problems or new processes.

3. Teaching and Learning Activities (TLAs)

(TLAs designed to facilitate students' achievement of the CILOs.)

TLA	Brief Description	CILO No.						Hours/week (if applicable)
		1	2	3				
Lecture	Introduction to CMOS technology	✓	✓	✓				3 hrs/wk (*Some of the lectures will be conducted in the laboratory)*
Tutorial	Key concepts are worked out based on questions and problem solving	✓	✓					
Laboratory	Lab sessions with hand-on experience, for the latest fabrication technology and device measurements techniques	✓	✓	✓				
Case study	Presentation and group discussion of various technology options	✓	✓	✓				

4. Assessment Tasks/Activities (ATs)

(ATs are designed to assess how well the students achieve the CILOs.)

Assessment Tasks/Activities	CILO No.						Weighting	Remarks
	1	2	3					
Continuous Assessment: 50%								
At least 3 assignments (assignments, case studies, laboratory experiments etc.)	✓	✓	✓				40%	
Test	✓	✓					10%	
Examination: 50% (duration: 2hrs , if applicable)								
							100%	

Remark:

To pass the course, students are required to achieve at least 30% in course work and 30% in the examination. Also, 75% laboratory attendance rate must be obtained.

5. Assessment Rubrics

(Grading of student achievements is based on student performance in assessment tasks/activities with the following rubrics.)

Applicable to students admitted in Semester A 2022/23 and thereafter

Assessment Task	Criterion	Excellent (A+, A, A-)	Good (B+, B,)	Marginal (B-, C+, C)	Failure (F)
1. Examination	Achievements in CILOs	High	Medium	Low	Not even reaching marginal level
2. Coursework	Achievements in CILOs	High	Medium	Low	Not even reaching marginal level

Applicable to students admitted before Semester A 2022/23

Assessment Task	Criterion	Excellent (A+, A, A-)	Good (B+, B, B-)	Fair (C+, C, C-)	Marginal (D)	Failure (F)
1. Examination	Achievements in CILOs	High	Significant	Moderate	Basic	Not even reaching marginal level
2. Coursework	Achievements in CILOs	High	Significant	Moderate	Basic	Not even reaching marginal level

6. Constructive Alignment with Programme Outcomes

PILO	How the course contribute to the specific PILO(s)
1, 2, 3, 4	This course aims to provide students with knowledge in advanced CMOS technology. Upon completion of this course, students will be able to describe current and anticipated trends in the CMOS technology, to evaluate and analyze the new technological options for advanced CMOS integrated circuit fabrication.
5,6	A mini project is allocated to allow students to practice this type of work which is directly linked to the methodologies learnt in the lectures. Students will be grouped into 2 and given a chance to practice the use of engineering tools in microelectronics and their communication skills in report writing and demonstrations.

Part III Other Information (more details can be provided separately in the teaching plan)

1. Keyword Syllabus

Syllabus discusses the topics of: CMOS Technology and Fabrication Processes, Nanoscale MOSFETs, Challenges of Giga-Scale Integration.

CMOS Technology Overview: Evolution and recent advances in silicon electronics, Moore's Law and the ITRS, State-of-the-Art CMOS technology.

Overview on Nano-CMOS Fabrication Processes: Overview of basic silicon processing steps, Sub-wavelength photolithography, Ultra-shallow junction fabrication, atomic layer deposition technique, plasma etching, advanced interconnects technologies.

Nanoscale MOSFETs:

MOSFET figures of merit: on and off current, CVI metric, gate delay, power-delay product.

Nanometer bulk MOSFETs: issues of downsizing, doping profiles, high-k dielectrics, gate stack design.

Non-classical MOSFET structures: transport enhanced MOSFETs (strained Si and SiGe, Ge), SOI MOSFETs, multiple gate MOSFETs (lateral double-gate MOSFET, FinFET, Tri-gate MOSFET).

Problems and challenges of nanoscale MOSFETs: performance degradation,, the limits of scaling (physical and process constraints).

Challenges of Giga-Scale Integration: Reliability and yield, interconnets and delay, power dissipation and thermal issues, economics issues, Si optoelectronic components.

2. Reading List

2.1 Compulsory Readings

(Compulsory readings can include books, book chapters, or journal/magazine articles. There are also collections of e-books, e-journals available from the CityU Library.)

1.	Guide to State-of-the-Art Electron Devices, IEEE Press and Wiley, 2012

2.2 Additional Readings

(Additional references for students to learn to expand their knowledge about the subject.)

1.	F. Schwierz, H. Wong, and J. J. Liou: Nanometer CMOS, (Pan Stanford Publishing, 2010)
2.	H. Wong, Nano-CMOS Gate Dielectric Engineering, (CRC Press, 2011)