City University of Hong Kong

Information on a Course offered by Department of Electronic Engineering with effect from Semester B 2012/13

Part I

Course Title:	Advanced CMOS Technology
Course Code:	EE 5430
Course Duration:	One Semester (13 weeks)
No. of credits:	3
Level:	P5
Medium of Instruction:	English
Prerequisite(s):	Nil
Precursors:	EE3115 Applied Optoelectronic Devices or EE3132 Microelectronic Circuit Designs
Equivalent Course:	Nil
Exclusive Courses:	Nil

Part II

Course Aims:

This course aims to provide the students with advanced CMOS technology knowledge required for VLSI circuits and system designs. Emphasis is placed on understanding the characteristics and limitations of nanoscale CMOS devices and the fabrication processes. The students will also be provided with hands-on experience in device designs and process simulations using the state-of-the-art CAD tools.

Course Intended Learning Outcomes (CILOs)
Upon successful completion of this course, students should be able to:

No.	CILOs
1.	Describe the processes and techniques used in nanoscale CMOS device and circuit fabrication.
2.	Understand the limitations and their solutions of nanoscale CMOS devices for gigascale integration.
3.	Derive the model equations for characterizing the short-channel effects, and figures of merit of nanoscale CMOS transistors.

Teaching and Learning Activities (TLAs)
(Indicative of likely activities and tasks designed to facilitate students' achievement of the CILOs. Final details will be provided to students in their first week of attendance in this course)

CILO 1	Lecture, tutorial, discussion, take home questions
CILO 2	Lecture, in-class exercise, discussion, case study
CILO 3	Lecture, laboratory, take home questions

Timetabling Information

Pattern	Hours
Lecture:	39*
Tutorials:	
Laboratory:	
Other activities:	

**Some of the lectures will be conducted in the laboratory.*

Assessment Tasks/Activities

(Indicative of likely activities and tasks designed to assess how well the students achieve the CILOs. Final details will be provided to students in their first week of attendance in this course)

	Type of assessment tasks	*Weighting (if applicable)*
Continuous Assessment	Case study, Assignments, Test, Lab experiments	50%
Examination	Written exam	50% 2 hours

Remarks: To pass the course, students are required to achieve at least 35% in course work and 35% in the examination. Also, 75% laboratory attendance rate must be obtained.

Grading of Student Achievement:

Letter Grade	Grade Point	Grade Definitions
A+ A A-	4.3 4.0 3.7	Excellent
B+ B B-	3.3 3.0 2.7	Good
C+ C C-	2.3 2.0 1.7	Adequate
D	1.0	Marginal
F	0.0	Failure

Constructive Alignment with Programme Outcomes

PILO	How the course contribute to the specific PILO(s)
1, 2, 3, 4	This course aims to provide students with knowledge in advanced CMOS technology. Upon completion of this course, students will be able to describe current and anticipated trends in the CMOS technology, to evaluate and analyze the new technological options for advanced CMOS integrated circuit fabrication.

5,6	A mini project is allocated to allow students to practice this type of work which is directly linked to the methodologies learnt in the lectures. Students will be grouped into 2 and given a chance to practice the use of engineering tools in microelectronics and their communication skills in report writing and demonstrations.

Part III
Keyword Syllabus:

Syllabus discusses the topics of: CMOS Technology and Fabrication Processes, Nanoscale MOSFETs, Challenges of Giga-Scale Integration.

CMOS Technology Overview : Evolution and recent advances in silicon electronics, Moore's Law and the ITRS, State-of-the-Art CMOS technology.

Overview on Nano-CMOS Fabrication Processes: Overview of basic silicon processing steps, Sub-wavelength photolithography, Ultra-shallow junction fabrication, atomic layer deposition technique, plasma etching, advanced interconnects technologies.

Nanoscale MOSFETs:

MOSFET figures of merit: on and off current, CVI metric, gate delay, power-delay product.

Nanometer bulk MOSFETs: issues of downsizing, doping profiles, high-k dielectrics, gate stack design.

Non-classical MOSFET structures: transport enhanced MOSFETs (strained Si and SiGe, Ge), SOI MOSFETs, multiple gate MOSFETs (lateral double-gate MOSFET, FinFET, Tri-gate MOSFET).

Problems and challenges of nanoscale MOSFETs: performance degradation,, the limits of scaling (physical and process constraints).

Challenges of Giga-Scale Integration: Reliability and yield, interconnets and delay, power dissipation and thermal issues, economics issues, Si optoelectronic components.

Recommended Reading:

F. Schwierz, H. Wong, and J. J. Liou: Nanometer CMOS, (Pan Stanford Publishing, 2010)

H. Wong, Nano-CMOS Gate Dielectric Engineering, (CRC Press, 2011)

S. Deleonibus: Electronic Devices Architectures for the Nano-CMOS Era - From Ultimate CMOS Scaling to Beyond CMOS devices, (Pan Stanford Publishing, 2008)

H. Iwai, Y. Nishi, M. Shur, and H. Wong: Frontiers in Electronics (Selected Topics in Electronics and Systems (vol. 41), (World Scientific, 2006).