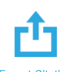
Journal of Applied Physics | ARTICLE | pubs.aip.org/aip/jap

Nonvolatile memory based on two-dimensional perovskite/organic polymer layered-heterojunction transistors

Cite as: J. Appl. Phys. **137**, 145501 (2025); doi: 10.1063/5.0241290
Submitted: 11 February 2025 · Accepted: 19 March 2025 ·
Published Online: 10 April 2025



Ni Zhou,[1,2] Liye Yang,[1] Liangyu Zhang,[1] Muhammad Irfan,[1] Ya Mo,[1] Paul K. Chu,[3] and Jia Li[1,a)]

AFFILIATIONS

[1]College of Engineering Physics, Shenzhen Technology University, Shenzhen 518118, China
[2]Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Shenzhen 518055, China
[3]Department of Physics, Department of Materials Science and Engineering, and Department of Biomedical Engineering, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China

[a)]**Author to whom correspondence should be addressed:** lijia@sztu.edu.cn

ABSTRACT

A nonvolatile memory device based on a layered-heterojunction transistor composed of two-dimensional Ruddlesden–Popper-phase perovskite and polymeric semiconducting films is fabricated. The intrinsic quantum wells in the two-dimensional perovskite act as charge-trapping layers to capture and store carriers when the device is biased, while the thin polymeric semiconducting film is the channel layer. The carrier transport and storage properties during gating are optimized, and the memory properties can be readily modulated. The memory device exhibits hysteresis transfer curves with a maximum storage window of 117 V and a current switching ratio of 10^2. The results reveal a simple and effective device structure and provide insights into the development of nonvolatile memory devices.

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I. INTRODUCTION

The rapid growth of information technology is placing increasing demand on high-performance nonvolatile memories (NVMs).[1–3] Among the various types of NVMs, the memory devices using field-effect transistors (FETs) as the building block are appealing due to non-destructive readout, ease of integration, and good compatibility with transistor-based applications.[4–6] Traditional FET-NVMs rely on the charge-trapping floating gates to store information with advantages such as long retention, high density, and low cost. However, device downscaling is reaching a limit rendering it difficult to maintain a small tunneling oxide thickness while minimizing the leakage current at the same time. Hence, attempts have been made to optimize the charge-trapping/transfer characteristics of FET-NVMs. For instance, semiconducting or metallic nanocrystals embedded in gate dielectrics have been shown to produce discrete charge-trapping sites, leading to reduced tunnel oxide thickness without sacrificing nonvolatility.[7] Alternatively, a high-k insulating layer can be implemented to exploit the charge-trapping capability, reduced coupling cross-talk, and good scalability.[8,9] FET-NVMs can be fabricated on capacity-based memories by taking advantage of the charge-trapping effect (CTE) to capture carriers and store information at the semiconductor–insulator interface, consequently improving the density, switching power, and speed.[10]

FETs showing the desirable charge dynamics in terms of trapping, transport, and dissipation while retaining decent electrical properties constitute a viable approach to designing high-performance NVMs. The organic heterojunction transistor (OHT) formed by combining specific charge-trapping materials with organic semiconductors is one possibility.[11,12] The charge dynamics of OHTs can be modulated by both electrical gating and interfacial charge trapping to produce distinctive electrical hysteresis and memory functions in conjunction with capitalizing on the organic-related merits in terms of flexibility, printability, lightness, and low cost.[13] It has been demonstrated that OHT-based memories can be prepared by reasonable materials selection and device structure design by coupling organic FETs with diverse

nanoparticles working as floating-gate charge-trapping materials, such as metals, metal oxides, carbon materials, and conjugated polymers.[14,15] These studies have provided important theoretical and experimental foundations for the development of memories based on organic thin-film transistors and suggested new ideas and methods to design high-performance non-volatile memories. Nonetheless, despite recent advances, the storage capacity, structural complexity, and processing difficulty must be improved prior to commercial acceptance.

Herein, a simple and effective device concept to design a high-capacity nonvolatile memory device based on a layered-heterojunction transistor composed of two-dimensional (2D) Ruddlesden–Popper-phase perovskite, phenylethylammonium lead bromide [$(PEA)_2PbBr_4$], is selected as illustrated in Fig. 1(a). The 2D Ruddlesden–Popper-phase perovskite, $(PEA)_2PbBr_4$, is selected because the naturally occurring organic–inorganic hybrid quantum-well (QW) structure [Figs. 1(b) and 1(d)] enables effective charge capture in the memory device. The p-type polymeric semiconductor, poly{2,2-(2,5-bis(2-octyldodecyl)-3,6-dioxo-2,3,5,6-tetrahydropyrrolo[3,4-c]pyrrole-1,4-diyl)-dithieno[3,2-b]thiophene-5,5-diyl-alt-thiophen-2,5-diyl} (PDPPBTT) composed of diketopyrrolopyrrole (DPP) and bisthienothiophene (BTT) shown in Fig. 1(c), exhibits the strong electron-withdrawing effects, thus producing efficient electron traps and benefiting memory applications.[16,17] In addition, PDPPBTT features high mobility and ease of solution processing,[18] and a high-quality conductive channel can be produced. By adopting this 2D perovskite/polymer heterostructure, the transistor has efficient charge-trapping/transfer characteristics, which can be readily modulated by electrical gating to yield the desirable memory properties. The memory device exhibits hysteresis transfer curves with a maximum storage window of 117 V and a current switching ratio of 10^2. The results reveal a simple device architecture that can be processed facilely for high-capacity FET-NVMs in information systems.

II. RESULTS AND DISCUSSION

The proof-of-concept device adopts the bottom-gate-top-contact transistor structure on the highly n-doped silicon wafers with a thermally grown SiO_2 insulating layer (n-Si/SiO_2), as shown in Fig. 1(a). In the fabrication, PEABr and $PbBr_2$ are dissolved in 1 ml of N,N-dimethylformamide (DMF) with a molar ratio of 2:1 to form a transparent precursor solution, and the 2D $(PEA)_2PbBr_4$ thin films are prepared by one-step spin coating. The p-type polymeric semiconductor PDPPBTT thin film is spin-coated on the 2D perovskite to form a channel layer. The Ti/Au source and drain

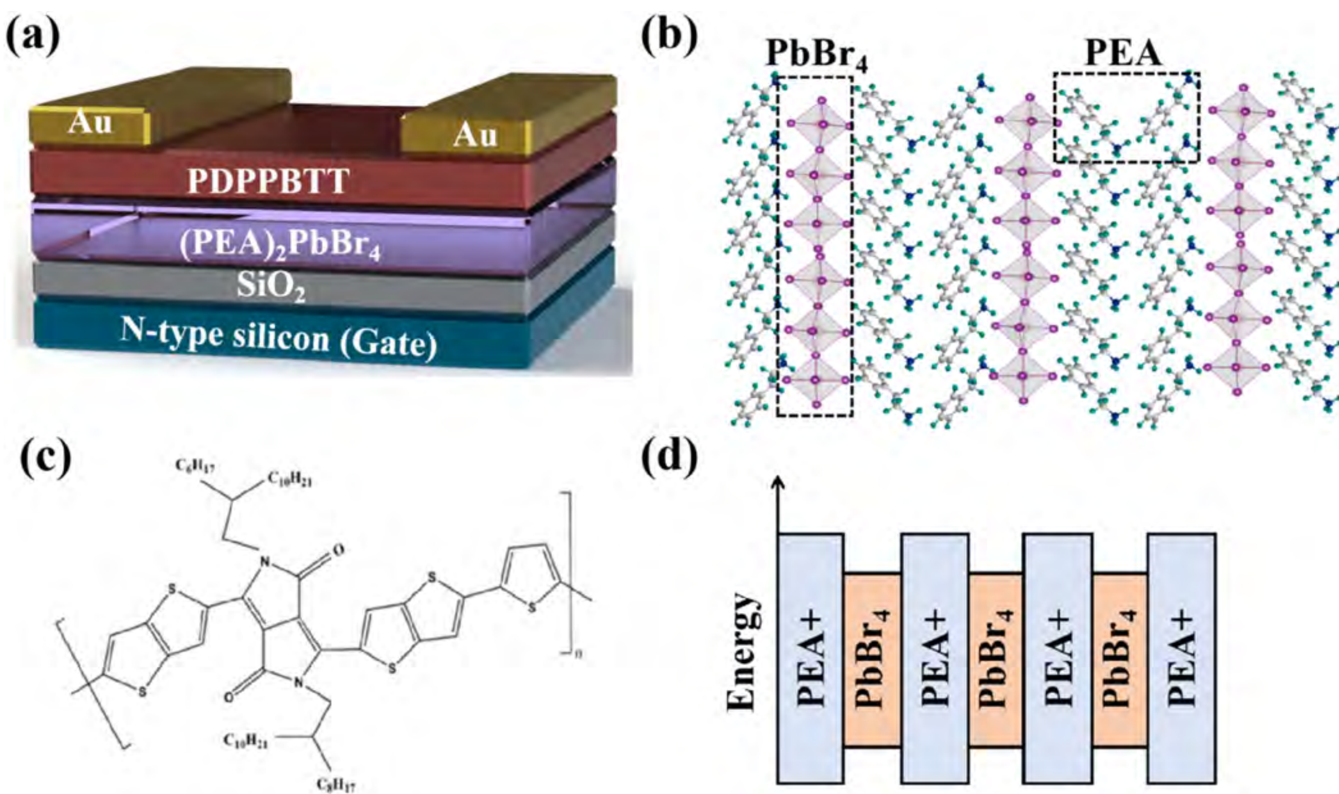

FIG. 1. (a) Structure of the memory transistor based on the 2D $(PEA)_2PbBr_4$/PDPPBTT heterojunction, (b) molecular structure of 2D $(PEA)_2PbBr_4$, which is a layered perovskite, (c) structure of PDPPBTT which is an organic polymer, and (d) schematic of the energy level of $(PEA)_2PbBr_4$.

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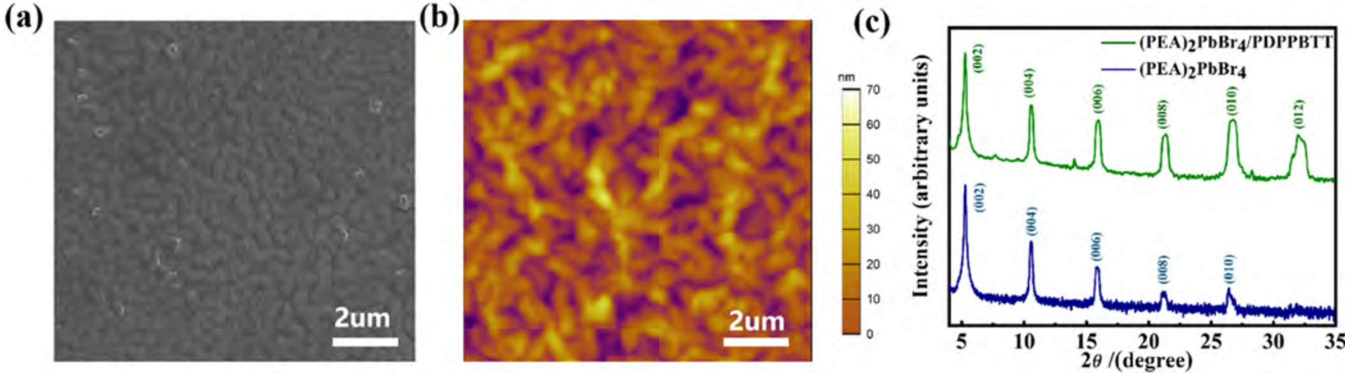

FIG. 2. (a) Top-view SEM image and (b) AFM image of $(PEA)_2PbBr_4$. (c) X-ray diffraction pattern of $(PEA)_2PbBr_4$ and $(PEA)_2PbBr_4$/PDPPBTT.

electrodes (5/60 nm) are then evaporated thermally on the PDPPBTT channel layer through a shadow mask.

Figure 1(b) depicts the crystal structure of 2D $(PEA)_2PbBr_4$, which consists of alternately stacked layers of inorganic $[PbBr_4]^{2-}$ octahedra and PEA^+ organic cations, forming a type-I quantum-well structure based on the bandgap difference. The morphology of the 2D $(PEA)_2PbBr_4$ film is examined by atomic force microscopy (AFM) and scanning electron microscopy (SEM) [Figs. 2(a) and 2(b)]. The SEM image shows that the $(PEA)_2PbBr_4$ film consists of platelet-like domains with pronounced and dense grains. AFM

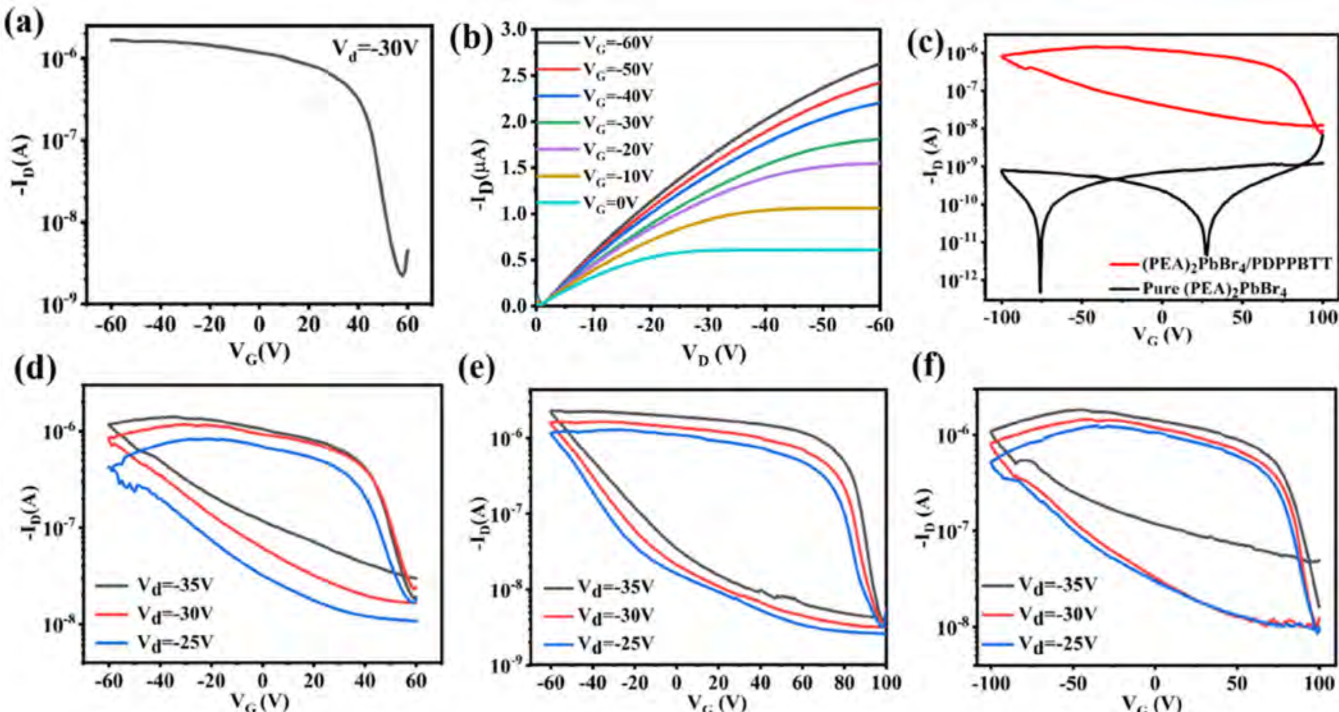

FIG. 3. (a) Transfer characteristics of the device composed of perovskite/organic heterojunction at $V_d = -30$ V, (b) output characteristics of the device under dark conditions, with V_G ranging from 0 to −60 V, (c) transfer cyclic characteristics of the device at $V_d = -30$ V based on $(PEA)_2PbBr_4$/PDPPBTT and pure $(PEA)_2PbBr_4$, (d) transfer cyclic characteristics of the device based on $(PEA)_2PbBr_4$/PDPPBTT heterojunction at $V_d = -25$, −30, and −35 V, with V_G ranging (d) from 60 to −60 V, (e) from 100 to −60 V, and (f) from 100 to −100 V.

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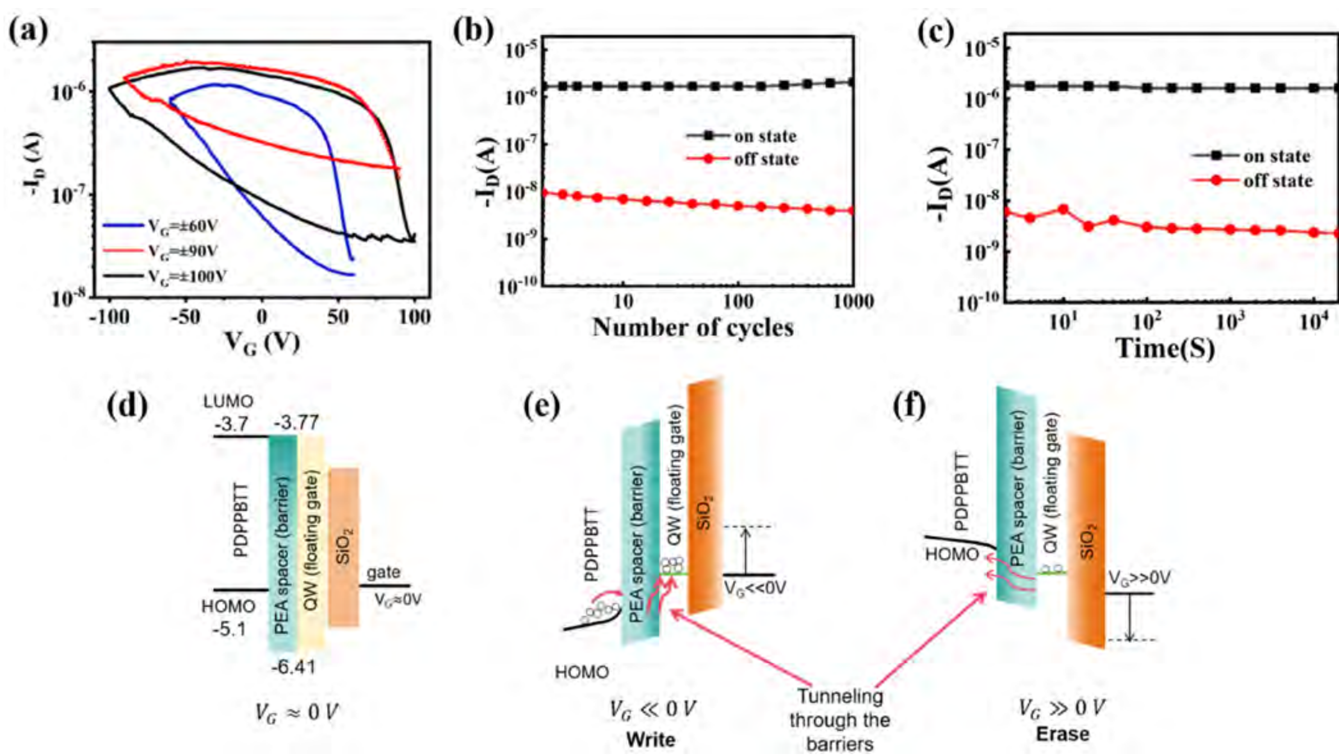

FIG. 4. (a) Variations of the hysteresis windows for V_G scanning ranges of ±60, ±90, and ±100 V with V_d = −30 V, (b) programming–erasing curves of the device for 10^3 cycles, (c) memory retention characteristics, and (d)–(f) energy band diagram of the perovskite/organic semiconductor floating-gate FET-NVM operating under different modes: (d) V_G = 0, (e) write, and (f) erase. Open circles represent hole charge carriers, HOMO and LUMO of perovskite are obtained by first-principles calculation.

reveals that $(PEA)_2PbBr_4$ is polycrystalline with a film thickness of approximately 70 nm. Figure 2(c) shows the x-ray diffraction (XRD) patterns of the $(PEA)_2PbBr_4$ film and $(PEA)_2PbBr_4$/PDPPBTT composite film. The evenly distributed diffraction peaks corresponding to (00L) (L = 2, 4, 6,…) indicate the successful formation of 2D Ruddlesden–Popper-phase perovskite.[19] Good crystallinity and highly selective crystal orientation are observed from 2D $(PEA)_2PbBr_4$. Furthermore, after PDPPBTT is coated, the diffraction peaks of the composite film are similar to those of the pristine perovskite, implying that the layered heterojunction formed by coating PDPPBTT does not distort the 2D Ruddlesden–Popper-phase structure.

The basic transistor characteristics of the FET-NVM device are determined. Figures 3(a) and 3(b) show the transfer and output characteristics of the FET device. The device shows the typical transfer characteristics of a P-type transistor with an on–off rate of $\sim 10^2$, implying that the carrier density can be modified by the gate voltage.[20,21] When the device is turned on, it exhibits the drain-current saturation behavior, as shown in Fig. 3(b), thereby providing direct evidence of the P-type channel transistor (V_G varied from 0 to −60 V). The feasibility of the 2D perovskite/polymer transistor is evaluated from the perspective of nonvolatile memory devices. The cyclic transfer curves of the transistor are shown in Fig. 3(c). The source-drain voltage V_d is fixed at −25 to −35 V, and the gate voltage V_G is forward-swept from +60 to −60 V and then back to +60 V. The transfer characteristics of the transistors exhibit a counterclockwise hysteresis in the channel current I_D giving rise to a prominent memory window. In contrast, the cyclic transfer curve of the pure 2D PVSK transistor does not show a hysteresis window and is in a non-conducting state, implying that the conduction channel is located in the PDPPBTT layer and hole accumulation occurs in the PDPPBTT atop the 2D PVSK.[11] In addition, the large hysteresis is maintained when the transistor is analyzed at different V_d [Figs. 3(d)–3(f)]. The influence of the applied gate field on the device hysteresis is evaluated by acquiring the transfer curves in the V_G sweeping ranges of ±60, ±90, and ±100 V at a constant V_d of −30 V [Fig. 4(a)]. The transfer characteristics also show a counterclockwise hysteresis storage window, which is enlarged with increasing sweeping V_G ranges, suggesting that the gate field plays a crucial role in affecting the hysteresis. The memory window can be evaluated by considering the shift of threshold voltages at writing and erasing states. In particular, the threshold voltages of −30 and 87 V can be obtained for the writing and erasing states, respectively, when the gate field is swept from +100 to −60 V and V_d is set to be −30 V (see Fig. S1 in the supplementary material). As a result, a maximum storage window of up to 117 V and a current switching ratio of 10^2 can be achieved. In addition, the hysteresis window shows a larger region of positive

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gate voltages compared to negative gate voltages, implying more electrons than holes in the trapped state. The counterclockwise hysteresis observed from the p-type channel transistor can be attributed to the charge-trapping effect. The intrinsic quantum-well structure in 2D $(PEA)_2PbBr_4$ plays the role of a floating gate where charge trapping/de-trapping occurs via quantum mechanical tunneling upon application of an electric field during device operation.[13,22,23]

The data retention time of the FET-NVM is evaluated using a write–read–erase–read cycle, in which "write" (ON) is triggered by applying a positive voltage pulse (70 V), while "erase" (OFF) is achieved by erasing the ON state with a negative voltage pulse (−70 V). The channel currents (I_{DS}) in the ON and OFF states are recorded as a function of time, as shown in Fig. 4(c). It is clear that the device is able to maintain stable programmed ON or OFF states after 10^4 s by applying V_G pulses of ±60 V in the write/erase operation. The device shows significant current differences after 10^3 write/erase cycles, suggesting stable fatigue characteristics of the device. The programming–erasing curve of the device is shown in Fig. 4(b). The OFF-state current is less stable during electrical erase, perhaps stemming from the instability of 2D $(PEA)_2PbBr_4$ under prolonged exposure to air.

The operation mechanism of our memory device is illustrated in Figs. 4(d)–4(f). The critical component of our FET device is the 2D PVSK/PDPPBTT layered heterostructure, in which the p-type polymer PDPPBTT acts as the transistor channel and 2D $(PEA)_2PbBr_4$ serves as the floating gate due to its intrinsic quantum-well structure. The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) of 2D perovskite material are determined by first-principle calculations (see the method part of supplementary material). During "writing" when a sufficiently high negative gate voltage is applied, holes accumulate in the PDPPBTT,[24] and the transistor is turned on. Under the gate electric field, the HOMO and LUMO levels shift up and undergo a certain degree of bending. The bending of the energy band facilitates the injection of holes from the PDPPBTT layer into the $PbBr_4$ quantum well by Fowler–Nordheim tunneling. Under the gating condition, the channel current increases and reaches the maximum ON current. The trapped charges in the floating gate form an opposite built-in electric field (E_{in}), which alters the distribution of carriers in the channel, consequently producing a negative shift in the transfer curve and threshold voltage V_{th}.[20,25] When the V_G bias is removed, the memory still retains the charge as the insulating barrier layers stop the trapped holes from escaping. When a positive gate voltage is applied, the hole concentration in the PDPPBTT channel decreases gradually, while the holes confined in the $PbBr_4$ QW are released to the PDPPBTT channel by the same tunneling process, causing the shift of the threshold voltage to a more positive value (erasing process). As the holes become fully depleted, the device is in the OFF state with the smallest channel current. The "read" operation is accomplished by applying a gate voltage between the erased and programmed threshold voltages, e.g., $V_G = 0$ V and recording the channel current flowing through the device. Therefore, the threshold voltage shifts during programming and erasing, and the memory effect can be monitored by the hysteresis window of the transfer curve during double V_G sweeping.

III. CONCLUSION

In summary, an FET-NVM device based on the 2D perovskite $(PEA)_2PbBr_4$ and polymer PDPPBTT layered heterostructure is demonstrated. By using PDPPBTT as the FET channel, the intrinsic quantum-well structure of 2D $(PEA)_2PbBr_4$ endows the device with efficient charge storage and transport during electrical gating to yield memory properties that can be readily modulated. The memory device exhibits hysteresis transfer curves with a maximum storage window of 117 V and a current switching ratio of 10^2. The results reveal a simple and effective device structure as well as a new concept for the development of nonvolatile memories with high application potential.

SUPPLEMENTARY MATERIAL

See supplementary material for more details about the experimental procedures, device characterization, calculation explanations, etc.

ACKNOWLEDGMENTS

The authors acknowledge support from the National Natural Science Foundation of China (Nos. 12474433 and 11974371), Key Area Funds of Universities of Guangdong Province (No. 2023ZDZX1021), Research Talent Start-Up Fund of SZTU (No. GDRC202140), Shenzhen Science and Technology Research Funding (Nos. JCYJ20220818101412027 and JCYJ20241202124900002), and City University of Hong Kong Donation Research Grants (Nos. DON-RMG 9229021 and 9220061).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Ni Zhou: Data curation (lead); Writing – original draft (lead). **Liye Yang:** Data curation (supporting). **Liangyu Zhang:** Data curation (supporting). **Muhammad Irfan:** Data curation (supporting). **Ya Mo:** Data curation (supporting). **Paul K. Chu:** Writing – review & editing (equal). **Jia Li:** Conceptualization (equal); Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and in the supplementary material.

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Supporting Materials

Nonvolatile memory based on two-dimensional perovskite/organic polymer layered-heterojunction transistors

Ni Zhou,[1,2] Liye Yang,[1] Liangyu Zhang,[1] Muhammad Irfan,[1] Ya Mo,[1] Paul K. Chu,[3] and Jia Li [1,a)]

[1] *College of Engineering Physics, Shenzhen Technology University, Shenzhen 518118, China*

[2] *Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Shenzhen 518055, China*

[3] *Department of Physics, Department of Materials Science and Engineering, and Department of Biomedical Engineering, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China*

[a)] *Author to whom correspondence should be addressed: lijia@sztu.edu.cn (J. Li)*

Experimental section

Materials: Lead(II) bromide ($PbBr_2$, 99.99%) and phenethylammonium bromide (PEABr, 99.5%) were purchased from Xi'an p-OLED Corp. N,N-dimethylformamide (DMF, anhydrous, 99.8%) and Chloroform ($CHCl_3$, 99.5%) were purchased from Aladdin. PDPPBTT was obtained from Luminescence Technology Corp. The $(PEA)_2PbBr_4$ precursor solution with the concentration of 0.2 M was prepared by dissolving 2:1 molar ratio of PEABr and $PbBr_2$ in DMF, and then stirred at 70℃ for more than 5 hours. The PDPPBTT solution was prepared using $CHCl_3$ with a concentration of 4.5 mg mL^{-1}. Both of them were filtered with 0.22 μm filter before use. All these processes were carried out in the glove box.

Device Fabrication: All devices were fabricated on the substrates of highly n-doped silicon (Si) wafers with a 200 nm-thick SiO_2. The substrates are cleaned with acetone, isopropanol and water for 20 min, respectively. Before spin coating, the substrates were first treated in a UV-ozone for 20 minutes. Then

the prepared perovskite solution was spin-coated at 2500 rpm for 40 s on a substrate and annealed at 100℃ for 10 min. Afterwards, the PDPPBTT solution was also spin-coated at 2500 rpm for 40 s on the perovskite film and annealed at 120 °C for 10 min acting as a channel. Finally, the source and drain electrodes were fabricated by thermally evaporating gold film on the device by using a shadow mask. The channel length (L) and width (W) of the devices were 50 and 1000 μm, respectively.

Characterizations: The UV-vis absorption spectra of the photoactive organic layer and perovskite layer were measured using UV-vis spectrophotometer from AOE instruments. The crystallinity of the films was characterized by XRD. All XRD spectra were obtained on a SmartLab X-ray diffractometer, Cu tube (CuKα =1.5418 A) and operated at 40 kV with a 2θ scan range of 3°–70°. The morphology and crystalline properties of the film are determined by scanning electron microscopy (SEM). All static electrical measurements were performed with a semiconductor parameters analyzer (PDA FS-Pro) in the dark at room temperature.

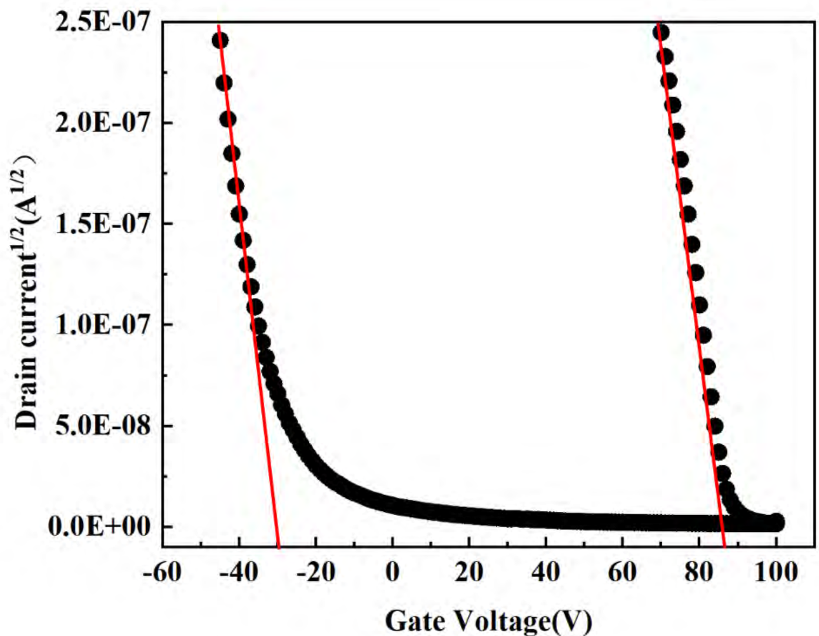

Fig. S1 Transfer curve used to evaluate the threshold voltages in writing and erasing states

Method about the first-principles calculations

First-principles calculations were performed using the most accurate hybrid exchange-correlation functional for band gap calculations, the generalized gradient approximation (GGA) functional, with predefined Perdew-Burke-Ernzerhof (PBE) parameters. Core electron effects were treated using pseudopotentials, as implemented in the density functional theory (DFT) package Quantum ATK. All calculations were conducted with a plane-wave basis set and a density mesh cutoff of 80 Ha. Dispersion interactions were accounted for using the Grimme-D3 method. A k-point grid of 4×4×4 was employed for sampling the Brillouin zone. For the molecular energy spectrum, absolute energy values were chosen instead of referencing to the Fermi level to provide a more accurate representation of molecular energy levels. The green dotted line represents the Fermi level, the black dotted lines indicates an unoccupied molecular orbital, and the solid black lines denotes an occupied molecular orbital. The Fermi level is -5.13 eV and the molecular band gap is measured between the lowest unoccupied molecular orbital (LUMO) -3.77 eV and the highest occupied molecular orbital (HOMO) -6.41 eV, as indicated by the arrow.

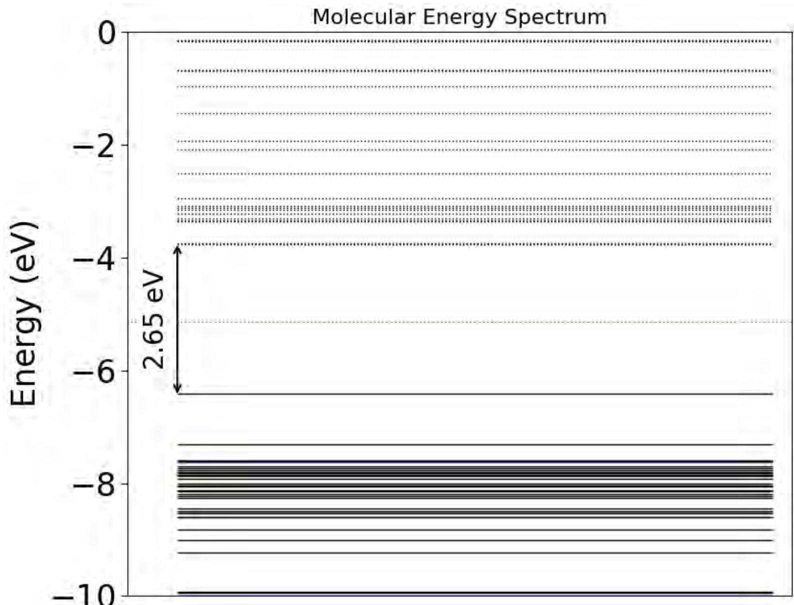

Fig. S2 Molecular energy spectrum of $(PEA)_2PbBr_4$, where the green dotted line represents the Fermi level, black dotted lines indicate unoccupied molecular orbitals, and solid black lines denote occupied molecular orbitals.