Nanotechnology 34 (2023) 015203 (9pp) https://doi.org/10.1088/1361-6528/ac96f5

Ambipolar steep-slope nanotransistors with Janus MoSSe/graphene heterostructures

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Received 11 May 2022, revised 4 September 2022
Accepted for publication 3 October 2022
Published 19 October 2022

Abstract

The transfer characteristics and switching mechanism of the steep-slope transistor composed of the graphene/Janus MoSSe heterostructure are investigated by quantum transport calculation. The Schottky barrier height at the Gr/SMoSe interface and tunneling width between the channel and drain can be tuned by the gate voltage, so that the device exhibits ambipolar switching with two minima in the subthreshold swing slope. 34 and 29 mV $decade^{-1}$ subthreshold swings can be achieved and the on/off ratios are over 10^6 and 10^8 for the different switching mechanisms. The device provides a solution and guidance for the future design of low-power, high-performance devices.

Keywords: Dirac source, steep-slope transistor, van der Waals heterostructures

(Some figures may appear in colour only in the online journal)

1. Introduction

Advances of electronic information processing systems with high power efficiency, area density, and switching speed have followed the trend of transistor downscaling based on Moore's Law [1]. In the past, scaling follows the 'Dennard scaling' principle in which the supply voltage is reduced in proportion to the geometric shrinking factor, such that the power density remains practically constant as the device area shrinks. However, lowering the supply voltage cannot catch up with reduction of the feature size leading to high power consumption and heat dissipation. This has become a major challenge for low-power nanoelectronics [2]. To overcome the power issue, an effective means is to design a steep-slope subthreshold swing (SS) transistor by maintaining a large ON/OFF current (I_{ON}/I_{OFF}) with a lower power supply [3, 4]. However, SS is hindered by the Boltzmann limit that cannot be below 60 mV $decade^{-1}$, thereby preventing continuous scaling of the operating voltage, OFF-state leakage current, area density, and overall power consumption consequently becoming a bottleneck of Moore's Law.

SS is defined by the gate voltage (V_{GS}), drain current (I_{DS}), and surface potential of the semiconductor as shown by the following equation:

$$\mathrm{SS} = \frac{\partial V_{GS}}{\partial(\log_{10} I_{DS})} = \frac{\partial V_{GS}}{\partial \Psi_S} \times \frac{\partial \Psi_S}{\partial(\log_{10} I_{DS})} = \left(1 + \frac{C_s}{C_{ox}}\right) \times \ln 10 \frac{kT}{q},$$

where $\partial V_G/\partial \Psi_S$ is the body factor, which is limited by the gate oxide and has a minimum of unity; $\partial \Psi_S/\partial(\log_{10} I_{DS}) = \ln 10kT/q$ is called transport factor, where $kT/q \approx 0.026$ eV at room temperature and is limited by the information carrier distribution in the source and transport process. Together, SS shows a minimum of 60 mV $decade^{-1}$ at room temperature. Based on the analysis of SS, various steep-slope transistors have been proposed. Tunneling FETs (TFETs) lower the transport factor by

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the band-to-band Zener tunneling effect at the electrode/channel interfaces, so that they can filter out the thermionic tail leading to steep SS [5–7]. However, TFETs usually suffer from low ON current (ION) limited by inter-band tunneling. Negative capacitance FETs (NCFETs) reduce the body factor via a ferroelectric gate layer with a negative differential capacitance [8–10]. The working states of NCFETs are unstable and large hysteresis of the current curves can be induced due to the different polarization states of the gate dielectric [11, 12].

The cold source (CS) FETs have emerged as a promising solution to overcome the limitations of T-FETs and NC-FETs [13, 14]. In CS FETs, the switching process is faster because the source carriers possess a more localized density-of-states distribution and have a shorter thermal tail, which can reduce the transport factor. Graphene (Gr) boasting the linear electronic dispersion has been chosen as the Dirac source (DS), one of the CSs, as it exhibits super-exponential decrease of the information carrier density by implementing proper doping. Liu *et al* have theoretically calculated the SS of Gr source-based FETs as follows:

$$\mathrm{SS} = \frac{\partial V_{\mathrm{G}}}{\partial \log_{10} I} \propto \frac{k_{\mathrm{B}} T \ln 10}{q}\left(1 - \frac{k_{\mathrm{B}} T}{E_{\mathrm{Dirac}} - \Phi_{\mathrm{B}}}\right).$$

If the Schottky-barrier Φ_B at the source/channel interface is below the Dirac point of Gr source, the transport factor will break the thermal limit. Except for a desired source, the source/channel interface can affect injection and gate tuning of a CS FET. Fortunately, a sharp Schottky-barrier with effective gate tuning can form at van der Waals (vdW) source/channel contacts due to the weak Fermi level pinning effect [15]. Therefore, CS FETs based on 2D vdW heterostructures have been proposed and studied experimentally and theoretically [13, 14, 16–22].

In this work, a steep-slope transistor based on the Gr/Janus MoSSe vdW heterostructure with Gr as the source and Janus MOSSs channel and drain is investigated. A Janus MoSSe can spontaneously dope Gr source due to the Janus doping effect, which facilitates the formation of a cold source [23, 24]. The switching mechanism and transfer characteristics of the device are simulated by self-consistent first-principles quantum transport calculation. Our results reveal that this device reduces the transport factor by not only self-filtering the thermionic tail with Gr Ds, but also tuning band-to-band tunneling at the channel-drain interface. Compared to other recently proposed cold-source devices, this device shows ambipolar transfer characteristics with double minima of SS of less than 60 mv decade^{-1} at room temperature.

2. Models and methods

Figure 1(a) shows the schematic of the device in which Gr is the source and the monolayer Janus MoSSe serves as the channel and drain. The vdWH of Gr and SMoSe in the overlap region ($L_{\mathrm{ov}} = 2$ nm) establishes a connection between source and channel. The current is controlled by a top and bottom gate of the same length L_{G} (8.6 nm) and ultrathin 3.2 nm HfO_2 is used as the gate oxide corresponding to an equivalent oxide thickness (EOT) of 0.5 nm SiO_2. The MoSSe drain is n-type doping with the concentration of 0.0026 e atom^{-1}, whereas MoSSe in the channel remains intrinsic. To produce a p-type Gr source, p-type doping with concentration of 0.06 e atom^{-1} is conducted. To illustrate the underlying mechanism and the fundamental advantages of the Gr source, we can deduce the carrier density why it is super-expotential. The carrier density $n(E)$ is defined as a product of the Fermi–Dirac distribution function $f(E) = 1/\{1 + \exp[(E - E_{\mathrm{F}})/k_{\mathrm{B}}T]\}$ and density of states DOS(E), where E_{F} is the Fermi energy. The general DOS(E) of d-dimensional materials is $D(E) = D_0(E - E_{c/v})^{\frac{d}{m}-1}$, where D_0 is constant, $E_{c/v}$ is the conduction/valance band (CB/VB) edge, k is the wave vector, $m = 2$ is for massive electrons and $m = 1$ for Dirac electrons. For 3D bulk semiconductors, normal 2D semiconductors, and Gr, the corresponding $n(E)$ can be expressed as $n_{3D}(\mathrm{E}) \propto \sqrt{E - E_C}\exp\left(\frac{E_{\mathrm{F}} - E}{kT}\right)$, $n_{2D}(E) \propto \exp\left(\frac{E_{\mathrm{F}} - E}{kT}\right)$, and $n_{\mathrm{Gr}}(E) \propto \sqrt{E_{\mathrm{Dirac}} - E}\exp\left(\frac{E_{\mathrm{F}} - E}{kT}\right)$ respectively. Asumming that $E_{\mathrm{F}} = 0$ eV, the carrier density of bulk and normal 2D materials follow the subexponential decay and exponential decay, both of which can produce a relatively long Boltzmann thermal tail at room temperature due to the Fermi–Dirac electron thermal excitation. Because of the long Boltzmann thermal tail, hot carriers can increase the leakage current by thermionic injection with energy higher than the channel barrier, causing the SS suffering from Boltzmann limit. Since Gr exhibits linear DOS (E), the $n(E)$ is superexponential decay when E_{Dirac}-E<1, which cause the thermal tail is quietly short and can be terminated at $E = E_{\mathrm{Dirac}}$ even at room temperature as show in figure 1(b). All in all, the Gr Dirac source can effectively reduce the leakage current and forms steeper SS.

The quantum transport properties are calculated by self-consistently solving Poisson's and Schrödinger's equations with the nonequilibrium Green's function formalism [25, 26]. The electrode temperature is 300 K and the real-space mesh cutoff is 105 Hartree. The K-point meshes for electrode region and central region are 30 × 1 × 85 and 30 × 1 × 1 in the x, y, and z directions, respectively. 240 × 1 k-point samplings in the x and y directions for the transmission and density of states calculation are the most favorable combination for the sake of more accurate results. The DFT-LDA method based on single electron approximation approaches the quasiparticle method and is accurate enough to describe the electronic structure of this case. The transmission coefficient $T(E, k)$ for a given k and energy E is obtained as:

$$T(E, k) = \mathrm{Tr}(G^{\mathrm{r}}(E, k) \cdot \Gamma_{\mathrm{S}}(E, k) \cdot G^{\mathrm{a}}(E, k) \cdot \Gamma_{\mathrm{D}}(E, k)],$$

where G^{r} and G^{a} are the retarded and advanced Green's function, respectively, and $\Gamma_{\mathrm{S/D}}(E, k)$ is the broadening width originating from the self-energy of source and drain.

The drain current I_{ds} is calculated by the Landauer–Bűttiker formula:

$$I_{\mathrm{ds}}(V_{\mathrm{ds}}, V_{\mathrm{gs}}) = \frac{2\mathrm{e}}{h}\int_{-\infty}^{+\infty}\{T(E, V_{\mathrm{ds}}, V_{\mathrm{gs}})[f_{\mathrm{s}}(E - \mu_{\mathrm{S}}) - f_{\mathrm{D}}(E - \mu_{\mathrm{D}})]\}dE,$$

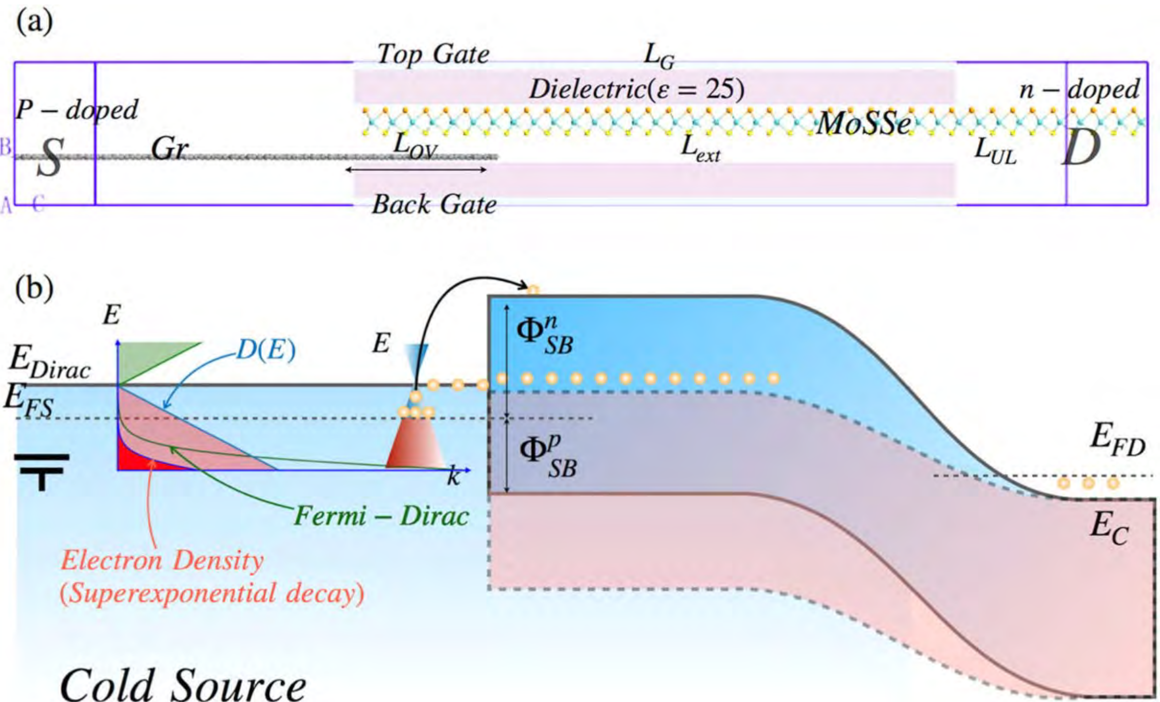

Figure 1. (a) Schematic structure of the DS FET and (b) Mechanism.

where f_S and f_D are the Fermi–Dirac distribution functions for the source and drain, respectively, μ_S and μ_D are Fermi levels of the source and drain, respectively. It should be noted that the transmission spectrum is kept from the bias voltage and gate voltage when one calculates the linear response current, meaning that the current only depends on the difference between f_S and f_D.

3. Results and discussion

The calculated lattice parameters of Gr and MoSSe are 2.46 and 3.22 Å, which are very close to the experimental measurements and previous theoretical results [27, 28]. MoSSe is a direct bandgap semiconductor with the CBM and VBM located on the high symmetry K point. The slight difference in the electronegativity of S and Se atoms produces a built-in dipole field with a potential difference of 0.66 eV pointing from S to Se.

To simulate the graphene/MoSSe heterostructure, a hexagonal supercell of graphene on top of MoSSe as shown in figure 2(a) is obtained with four and seven repetitions of the MoSSe and graphene unit cells, respectively. Since the MoSSe monolayer has different atoms (S or Se) on each side, two types of stacking configurations of graphene on MoSSe are formed, labeled as G/SMoSe and G/SeMoS heterostructures. Since Gr in Gr/SMoSe can be spontaneously p-doped, Gr/SMoSe is chosen as the electrode for better n-type Dirac source. As show in figure 2, Gr and SMoSe are twisted by 13.8°. Figure 2(d) shows the projected band structures of the G/SMoSe heterostructures, in which the contributions from graphene and the MoSSe monolayers are denoted by red lines and blue lines, respectively. The band structure can be approximated by the simple combination of Gr and SMoSe. As for graphene, the linear Dirac-like dispersion relationship around the Fermi level is well preserved and the Dirac points are slightly over the Fermi level due to the Janus doping effects. The bands contributed by the MoSSe layer demonstrate that the direct semiconductor characteristics are retained. The bandgap of the MoSSe layer is 1.72 eV for the G/SMoSe heterostructures and almost unchanged compared to the pristine MoSSe monolayer. In the Gr/SMoSe system, it is clear that the Fermi level is close to the CBM of the MoSSe layer consequently forming an n-type Schottky contact with a small Schottky barrier (SB) height of 0.5 eV. The SB height is located at the (1/3, 0,0) point.

Based on the electronic structure of Gr/SMoSe vdWH, a double gate Gr/SMoSe FET is constructed. Overall, this device differs from that of a monolayer-based double-gate MOSFET only by the presence of a source injector coupled to the channel. To check the Dirac source and gate tunable SB height, the eequilibrium transport is derived. Figures 3(a)–(c) show that a Schottky barrier is formed at the Gr/SMoSe interface and the height of the n-type source-channel SB is gate-tunable with a low barrier height for easy electron injection in the ON state and high barrier height to block electron injection in the OFF state. Specifically, as the gate voltage increases, the n-type SB height decreases and the CBM crosses the Dirac point of the Gr source. As the gate voltage decreases to a negative value, VBM of the MoSSe channel is pushed up and the tunneling width of channel to drain also be tuned to be narrower thus acting like a TFET. Hence, the channel barriers consist of the SB at source/channel interface as well as band-to-band tunneling (BTBT) at channel/drain interface. These two-gate tunable conductive variables imply ambipolar transfer characteristics. Figures 3(d)–(f) show

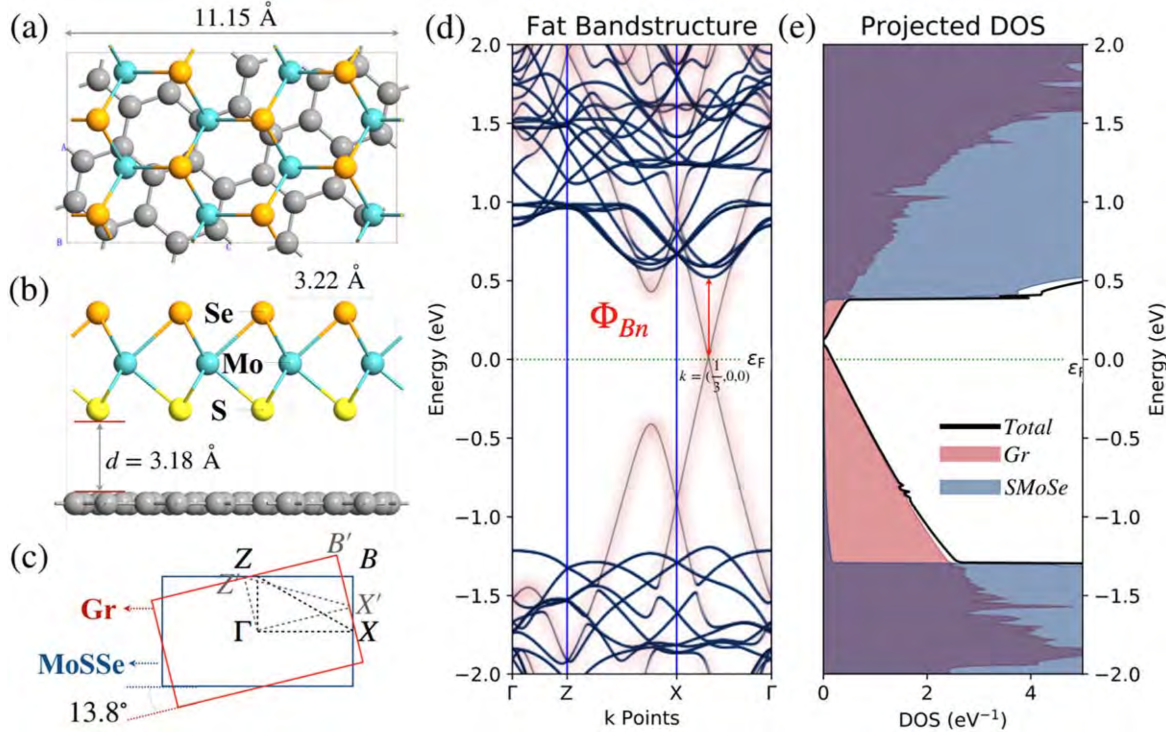

Figure 2. (a) Top view of Gr/SMoSe vdWH; (b) side view; (c) Brillouin zone with high-symmetry points labeled; (d) projected band structure of the Gr/SMoSe vdW heterostructure with red representing Gr and blue representing SMoSe; (e) PDOS of Gr/SMoSe vdWH.

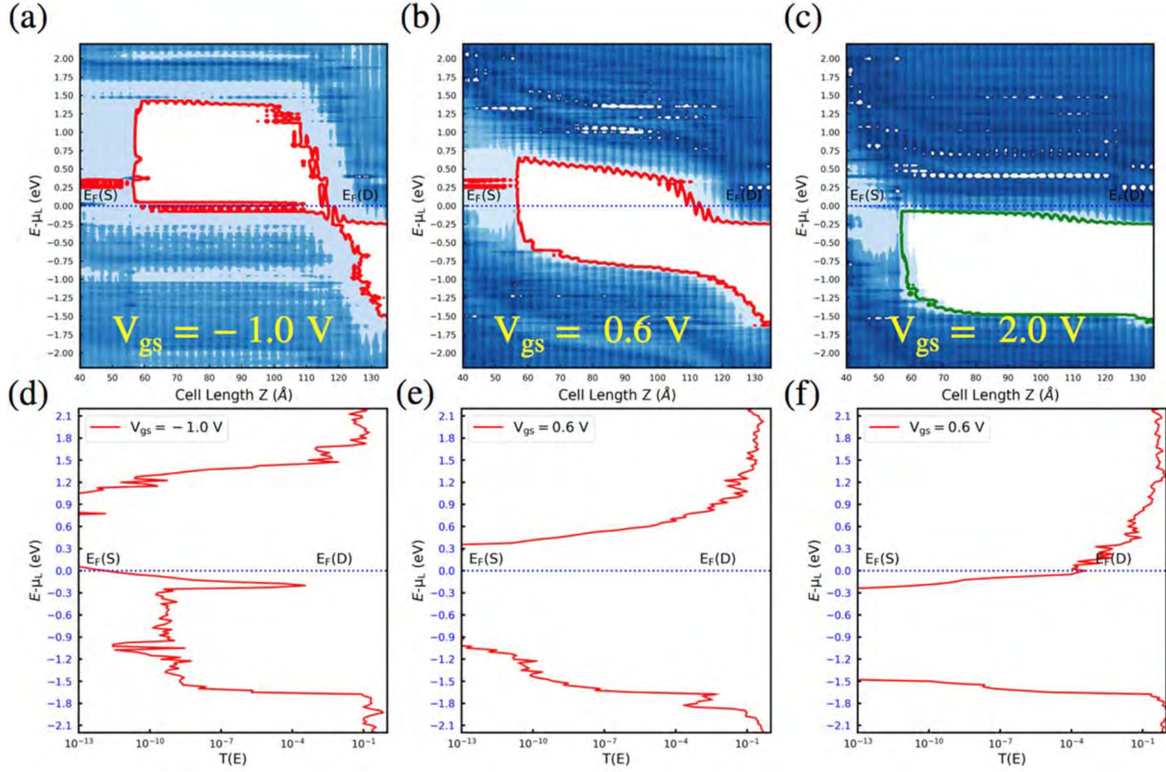

Figure 3. (a)–(c) PLDOS of the device at different gate voltages and (d)–(f) Transmission spectra corresponding to the PLDOS.

the transmission spectra of the device for different V_{gs}. As expected, there is significant contrast of the transmission probability at the Fermi level of the source between the ON and OFF states due to the change of the channel barrier.

The nonequilibrium transport characteristics at different supply voltages and gate voltages are then analyzed. The characteristics at $V_{ds} = 0.1$ and 0.5 V are plotted in figure 4(a) as shown by the cyan and blue lines, respectively. The curve

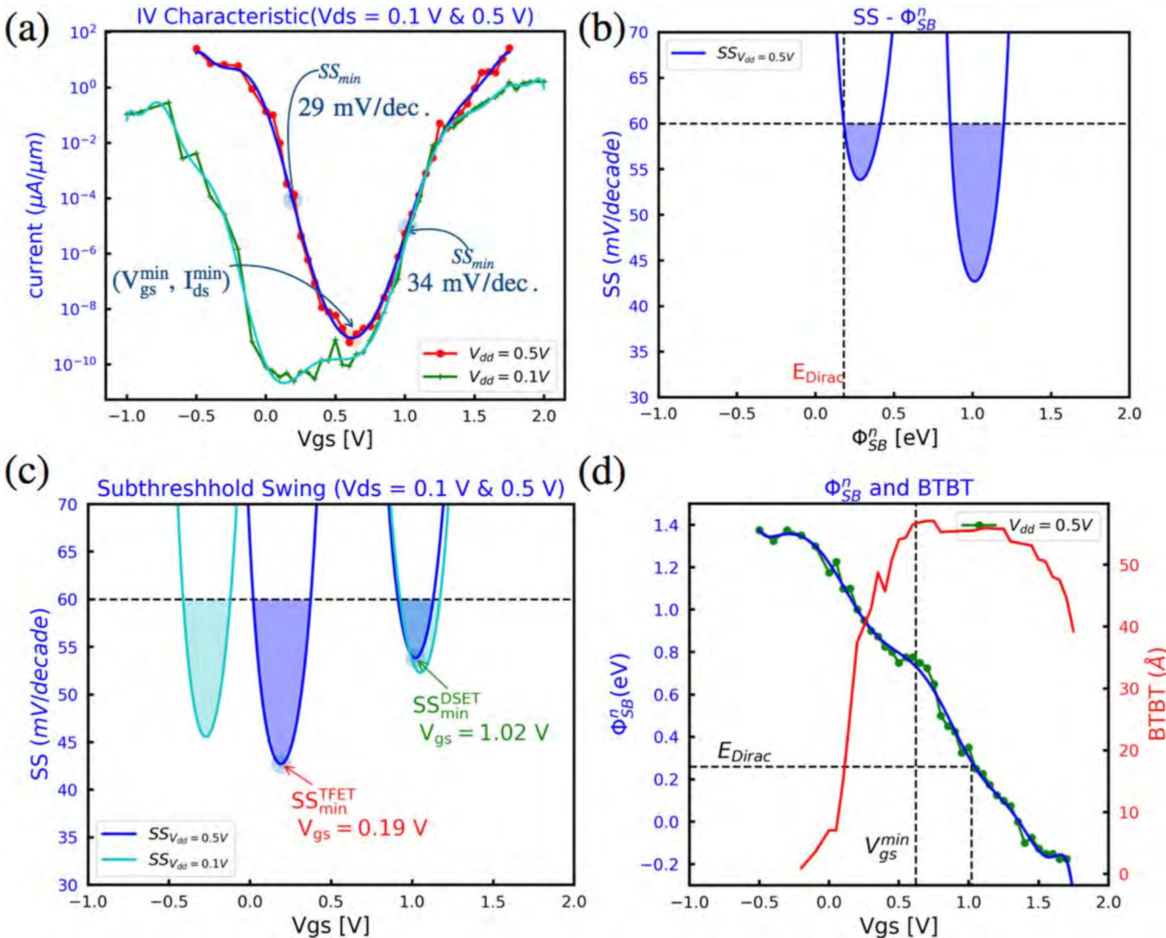

Figure 4. (a) Transfer characteristic curves at $V_{ds} = 0.1$ and 0.5 V; (b) SS as a function of SB at the Gr:SMoSe interface; (c) SS as a function of the gate voltage for $V_{ds} = 0.1$ and 0.5 V; (d) height of SB at the Gr:SMoSe interface and width of the tunneling barrier at the channel-drain interface as functions of the gate voltage.

is first studied for $V_{ds} = 0.5$ V. The transfer curve exhibits a clear ambipolar behavior with an electron–hole asymmetry as predicted by the equilibrium band diagram and prevailing n-type conduction in high voltage. There is a minimum conduction point (V_{gs}^{min}, I_{ds}^{min}) seperating the electron conduction ($V_{gs} > V_{gs}^{min}$) from the hole conduction ($V_{gs} < V_{gs}^{min}$). The minimum point should shift with the device structure parameters and supply voltages. Consequently, a 34 mV decade^{-1} minimum SS in the DS FET region and 29 mV decade^{-1} minimum in the TFET region are observed. Table 1 compares our results with those of other DS FETs based on Gr/MoS_2, Gr/CNT, and Gr/InSe. Although Gr/CNT also shows clear ambipolarity in the transfer characteristic curve, the mechanism of the ambipolarity is not clear compared to the description in this paper.

The IV characteristics can be divided in two sections, ($V_{gs} > V_{gs}^{min}$) and ($V_{gs} < V_{gs}^{min}$). To make more specific analysis, the transfer curves are fitted. The fitted I_{ds}–V_{gs} curve in figure 3(a) shows that V_{gs}^{min} is near 0.6 V under $V_{ds} = 0.5$ V. Furthermore, when the device works in the DS FET region, a sub-60 mV decade^{-1} spans three decades when V_{gs} changes from 0.9 to 1.1 V and spans six decades when it works in the TFET region with V_{gs} decreasing from 0.3 to 0.0 V. If $V_{gs}^{off} = 0.8$ V for the DS FET mode, $V_{gs}^{on} = V_{gs}^{off} + V_{DS} = 1.3$ V, the on/off ratio is more than 10^6, $V_{gs}^{off} = 0.45$ V for the TFET mode, $V_{gs}^{on} = V_{gs}^{off} - V_{DS} = -0.05$ V, and the on/off ratio is near 10^8.

To explore the switching mechanism of this device, the band diagram along the transport direction of the device is extracted from the PLDOS results in figure 5(a) and the corresponding transmission spectrum and spectral current are presented in figures 5(b) and (c). Figure 5(d) shows that the density of states of the source, channel and drain are changed by V_{gs}. The SB height at Gr:MoSSe interface is calculated and the BTBT width between the channel and drain is tuned by V_{gs}, as shown in figure 4(d). The SB height can be tuned by V_{gs} near linearly with a slope about -0.88 eV V^{-1} and Φ_{SB} crosses the Dirac point at V_{gs} of about 1.0 V. The BTBT width decreases quickly when V_{gs} changes from 0.3 to 0.0 V. Figure 4(d) shows that when V_{gs} is near 0.6 V, the BTBT width is the largest thus preventing channel hole tunneling to the drain. The height of the Gr:SMoSe interface is far from E_{Dirac} implying that Dirac electrons cannot contribute to the current and therefore, the current reaches a minimum at 0.6 V.

When V_{gs} is increased from 0.6 V, the device works in the DS FET region. The current is mainly contributed by thermionic electrons near the Dirac point of the Gr source,

Table 1. Comparison of different DS FETs.

	$SS_{mim(DSFET)}$ [mV dec^{-1}]	$SS_{mim(TFET)}$ [mV dec^{-1}]	L_g [nm]	L_{UL} [nm]	EOT [nm]	V_{ds} [V]	I_{on} /I_{off}	τ [ps]	PDP [fJ μm^{-1}]
Gr/SMoSe(sim.)	34	29	8.6	4	0.5	0.5/0.1	$10^6/10^8$	0.02(TFET) 3.5 (DS FET)	0.078(TFET) 0.061 (DS FET)
Gr/MoS_2(sim.) [13]	30	/	14.6	5	0.5	0.3	10^6	5	/
Gr/InSe(sim.) [18]	51	/	7.8	5	0.54	0.74	10^9	/	/
Gr/CNT(exp.) [14]	35	/	15	4	1.5	0.5/0.1	10^6	/	/
Gr/MoS_2(exp.) [17]	29	/	/	5	/	0.1	10^7	/	/
ITRS 2022	102	/	8.8	5	0.49	0.69	10^3	0.567	0.285

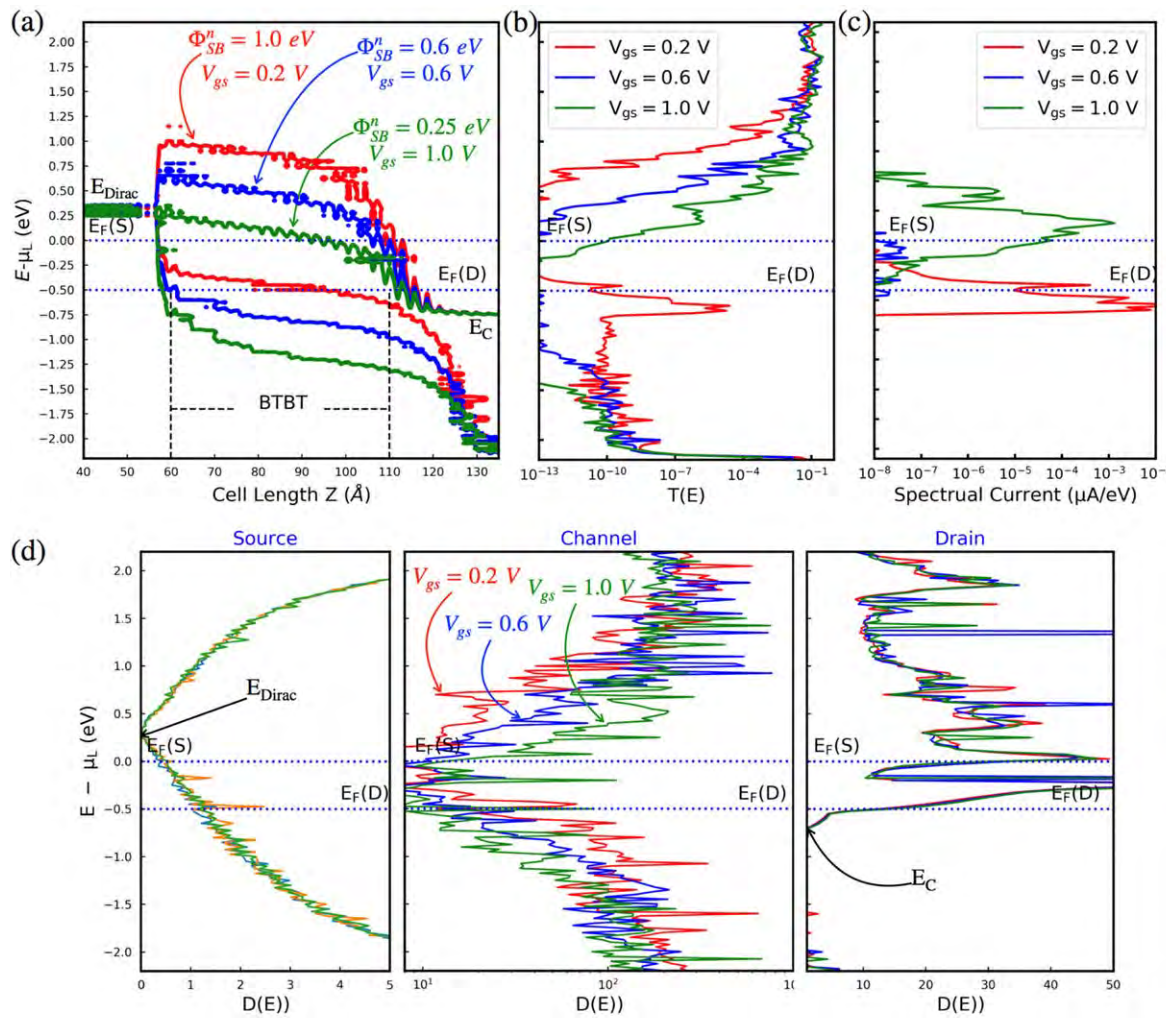

Figure 5. (a) Band diagram extracted from PLDOS for $V_{gs} = 0.6$ V, 0.2 V and 1.0 V; (b) and (c) transmission spectra and spectral currents of (a); (d) device DOSs projected to the Gr source, channel, and drain for V_{gs}^{min} and subthreshold voltages of DS FET and TFET at $V_{gs} = 0.2$ and 1.0 V.

which is tuned by the SB height. As V_{gs} increases continuously, the SB height decreases and the width of BTBT at channel/drain interface increases. The SB blocks the Dirac electrons due to the short thermal tail effect and the tunneling barrier prevents the tunneling current. As a result, the leakage current is small when Φ_{SB} is greater than E_{Dirac}. However, when V_{gs} is greater than 1.02 V, Φ_{SB} is lower than E_{Dirac}. The drain current becomes large suddenly and SS reaches a minimum, corresponding to SS_{min} in figures 4(a)–(c).

When V_{gs} is decreased from 0.6 to −0.5 V, the device works in the TFET region. The current stems entirely from tunneling and is mainly controlled by the BTBT width between the MoSSe channel and MoSSe drain. Figure 3(d) shows that the barrier width changes rapidly in the range of 0.0–0.3 V and this is the main reason why the device SS is small. The uniqueness of this device is that in the current window, the leakage tunnel current is controlled by both the p-type SB and tunneling barrier between the channel and drain. Since V_{gs} can reduce the p-type SB height and width of the tunneling barrier, the drain current rises quickly making SS small. Figure 4(c) shows that when $V_{gs} = 0.19$ V, SS reaches the minimum and the BTBT width changes quickly in the vicinity of this voltage as shown in figure 4(d).

To study the scaling behavior of the supply voltage, the transfer curve for $V_{ds} = 0.1$ V is studied. The curve remains ambipolar. In the DS FET region, the subthreshold switching process basically overlaps for $V_{ds} = 0.5$ V, except that the on current is smaller. Besides, the SS_{min} of the DS FET is slightly lower than $V_{ds} = 0.5$ V, meaning that the device can be further downscaled without losing the switching speed in this working mode. In the TFET region, the leakage current decreases over five grades because the current is contributed entirely by tunneling. Meanwhile, the SS_{min} of TFET becomes larger. Overall, there is a tradeoff between the performance of the DS FET and TFET when the supply voltage and feature size are scaled down.

Since the performance of the DS FET and TFET is affected by different factors, shortening the gate length and overlapping length of Gr/SMoSe can improve the on current, but will not affect the DS FET performance because the SB height is a key factor of the DS FET. However, the off-state leakage current of the TFET increases and it is not preferred.

The proper underlap length between the gate and drain can further improve the characteristics of the DS FET and TFET modes. In addition, the supply voltage needs to be optimized to make the SS steeper and on-state current larger.

To further assess the device characteristics, the switching speed is characterized by the intrinsic delay, which is calculated by $\tau = (Q_{ON} - Q_{OFF})/I_{ON}$, where Q_{ON} and Q_{OFF} are the channel charges at ON- and OFF-state, respectively. The power consumption is measured by the power–delay product (PDP) which is estimated as PDP $= (Q_{ON} - Q_{OFF})V_{ds}$. If I_{on} is effectively defined, τ and PDP can be determined. The calculated τ values of the Gr/SMoSe device are 0.02 ps for TFET and 3.5 ps for DS FET and the PDP values are 0.078 fJ μm^{-1} for TFET and 0.061 fJ μm^{-1} for DS FET.

4. Conclusion

In summary, a Gr/SMoSe nanotransistor can be controlled by the height of the Schottky barrier at the source/channel interface and the tunneling width between channel and drain, both of which can be effectively regulated by the gate voltage, giving rise to an ambipolar characteristics. When the device is operated in the DS FET mode, SS_{mim} can reach 34 mV decade^{-1} and sub-60 mv decade^{-1} spanning three decades can be achieved. The on/off ratio exceeds 10^6. When the device works in the TFET mode, a minimum SS of 29 mV decade^{-1} can be accomplished and sub-60 mV decade^{-1} for more than six decades with the on/off ratio near 10^8 is observed. Moreover, the feature size and supply voltage can be reduced further while preserving the switching characteristics. Above all, this device provides a solution for the future design of low-power, high-performance devices as a possible way to continue the Moore's Law.

Acknowledgments

This research was supported by the National Natural Science Foundation of China (Grant Nos. 51872010, 61975005), Foundation of Beijing Academy of Quantum Information Sciences (Grant No. Y18G28), City University of Hong Kong Donation Research Grant (DON-RMG 9229021), City University of Hong Kong Donation Grant (9220061), as well as Hong Kong ITC (Innovation and Technology Commission) ITF (Innovation and Technology Fund) (GHP/149/20SZ and CityU 9440296).

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Conflict of interest

The authors declare no conflict of interest.

Availability of data

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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