Recent Progress in Patterned Silicon Nanowire Arrays: Fabrication, Properties and Applications

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Abstract: Currently there is great interest in patterned silicon nanowire arrays and applications. The accurately controlled fabrication of patterned silicon nanowire arrays with the desirable axial crystallographic orientation using simpler and quicker ways is very desirable and of great importance to material synthesis and future nanoscale optoelectronic devices that employ silicon. The recent advances in manipulating patterned silicon nanowire arrays and patents are reviewed with a focus on the progress of nanowire fabrication and applications.

Keywords: Patterned silicon nanowire arrays, chemical vapor deposition, molecular beam epitaxy, thermal evaporation, self-selective electroless plating, Si solar cells, thermal conductivity, field-effect transistor.

INTRODUCTION

A great deal of effort has been made in the recent years to fabricate a variety of semiconducting nanostructures [1, 2]. Among them, silicon is the most important semiconducting material, and silicon nanowires (SiNWs) have attracted considerable attention due to their potential application in nanoscale electronic and optoelectronic devices [3-6]. Compared to bulk silicon, SiNWs show some special physical properties including field emission [7-9], thermal conductivity [10-13] and photoluminescence [14-17]. Many SiNWs-based nanodevices have been demonstrated as field-effect transistors (FET) [18-26], biological and chemical sensors [27-31] and solar cells [32-45]. Usually, SiNWs are growing with random orientations and irregular diameters. But now patterned silicon nanowire arrays (PSNA) fabricated by some conventional methods grasp more and more researchers’ interest for their controlled size, orientation, and packing density [46, 47]. This review focuses on the progress and advance in the fabrication, properties and applications of PSNA, with an emphasis on future challenges.

FABRICATION

There are two basic approaches of synthesizing PSNA: top-down and bottom-up approach. Top-down approach can be linked to sculpting from a block of stone. In the top-down approach, a large piece of silicon is cut down to smaller pieces through different means, such as dry or wet etching and lithography. In contrast, the bottom-up approach can be linked to building a brick house. The nanowire is synthesized by the combination of silicon atoms. The representative methods are chemical vapor deposition (CVD), physical vapor deposition (PVD) and molecular beam epitaxy (MBE).

For a typical top-down method [48], PSNA has been fabricated with low-cost and high throughput by a catalytic template etching process. In this process, the diameter, height of individual nanowires, and the center-to-center distance between nanowires have been accurately controlled. The overall fabrication process is described in the following. First, a monolayer of polystyrene sphere is allowed to selfassemble on a silicon substrate like the template. Then the diameter of the polystyrene spheres is reduced by a reactive ion etching process. Second, a silver film is thermally evaporated onto the silicon substrate as a catalyst Owing to the polystyrene monolayer mask, a silver film with a hexagonal array of holes is formed. Third, the substrate immerses in an aqueous HF solution contains H₂O₂. The Ag film catalyzes the etching of silicon beneath it. Finally, the polystyrene spheres are removed by dissolution in CHCl₃ and the Ag film is dissolved in boiling aqua regia.

In contrast to the etching techniques used in the top-down methodology, the bottom-up approach involves the direct growth of nanowires on the substrate. For instance, SiNWs were successfully fabricated by thermal evaporation of silicon wafer at high temperature by solid-liquid-solid mechanism [49]. In the beginning, the silicon wafers are covered with gold particles produced by electrochemical method using AuCl₃ solution. And then they are placed in a quartz boat which is put in the center of a horizontal quartz tube furnace. SiNWs are generated by means of a low-vacuum CVD system. The temperature of silicon-metal alloy droplets can be divided into several ranges. In the droplet, the temperature from the bottom to the top decreases gradually (a→b→c→d→e→f). Therefore, the saturation concentration of silicon at the bottom of the alloy is highest while in the top is lowest. During the process of SiNW formation, the top region (f) reaches supersaturation firstly so that some silicon atoms are precipitated out of the droplet to upward side. Next, silicon atoms in region (e) transfer to region (f) because of the concentration gradient. As the picture shows, Si
atoms originating from the silicon substrate transfer continuously from region (a) to the region (f). Si atoms arrange themselves as required, and finally SiNWs grow upward.

Among all synthesis methods, vapor-liquid-solid (VLS) process seems to be the most popular one as bottom-up approach [50]. This process was originally developed by Wanger and Ellis to prepare silicon whiskers in 1960s [51]. At that time, such structures in the range of micrometers were defined as “whiskers”. The VLS process can be divided into two main steps: (1) the formation of a small liquid droplet (2) the alloying, nucleation, and growth of the nanowire [52].

Recently, many research groups generated PSNA based on the VLS growth mechanism. According to the different growth techniques, we can further classify the fabrication process into CVD [53-57], thermal evaporation [58], MBE [59-61] and so on.

**Chemical Vapor Deposition**

CVD is a technology that uses gaseous or vaporous materials growing solid sediments in gas phase or gas-solid interface. This technology usually puts the silicon wafers which covered with metal nanoparticles into a quartz reaction vessel, utilizes SiCl$_4$ or SiH$_4$ (H$_2$ or N$_2$ is often used as the carrier gas) as the precursor in a certain temperature and vacuum; grows SiNWs on the substrate [62]. The basic process of forming SiNWs include gas diffusion, reaction gas adsorption in the substrate, surface reaction, nucleation and growth, then gas desorption and volatilization etc.

Yang and co-workers successfully grew vertically PSNA on Si substrates with precise controlled diameter, density and spatial distribution using directed gold colloids for VLS-CVD [63]. As shown in Fig. (1), a poly (dimethylsiloxane) (PDMS) stamp is made using a photoresist as master, and then it is “inked” with the poly-L-lysine solution. The patterned substrate is immersed in the Au colloid solution which is formed by transferring the patterned polymer to the substrate at 70 °C for 5 min. Only the Si surface is with a thin layer of a polyelectrolyte and can adhere the Au colloids and the polymer disappears during the growth of SiNWs. The gold colloids are used to define the diameter and position of the SiNWs and SiCl$_4$ is used as the precursor molecule. Au colloids act as the seeding metal because its diameter precisely controls the nanowire diameter. The growth density is controlled by the concentration of the colloid solution. In this way we can obtain different PSNA by changing the patterned substrate and the parameter of the Au colloid solution. The main difficulty of this process is how to control the location of the Au nanocrystals on the substrate.

In order to effectively control the location of the Au nanoparticles and fabricate the ordered single crystalline PSNA, many researchers used nanochannel alumina as templates and synthesized PSNA by CVD process [64-67]. The templates are prepared by anodizing high-purity aluminum foils in acid solutions through a two-step anodization method. The templates are bestrewn with ordered hexagonally pores, and the average diameter of pores can be changed by different anodization voltage. At first, gold particles are deposited at the bottom of the hexagonal holes keeping the gold particles with the size and morphology of the

![Fig. (1). Schematic of PDMS patterning of Au colloids. Reprinted with permission from [63]. Copyright 2005 by American Chemical Society.](image-url)
holes. Then silane is paralyzed with the catalytic, ordered single crystalline SiNWs are synthesized successfully. The diameter of the nanowires depends on the size of the template holes.

**Molecular Beam Epitaxy**

MBE is also an effective method for preparing PSNA [59-61]. For instance, Fuhrmann and co-workers produced PSNA by nanosphere lithography and MBE [60]. In the process, two main steps have to be realized: i) regularly arranged gold islands in the nanometer range were formed by an inexpensive, simple and fast lithography tool named nanosphere lithography; ii) PSNA were grown by MBE gold templates produced with polystyrene particles.

Compared to the previous experiments [59], the best improvement is that the nanowires have no sharp size distribution because the utilization of nanosphere lithography. Fig. (2) illustrates the fabrication steps of PSNA. (a) Polystyrene particles deposited on a Si substrate which was covered by an oxide layer forming monolayer; (b) Gold was deposited in the triangular holes of the polystyrene layer by thermal evaporation; (c) The polystyrene layer was removed from the substrate by two steps: (i) CH₂Cl₂ in an ultrasonic bath for 2 min (ii) washing in acetone, ethanol and water; (d) The substrates were heated at 810 °C for 10 min to remove the native oxide layer and also transformed the triangular gold islands into hemispheres; (e) Silicon deposited and nanowires growth started as the temperature in the range of 525 to 570 °C by MBE.

**Thermal Evaporation**

The method of thermal evaporation and laser ablation was applied for the preparation of SiNWs almost at the same time. As is similar to the laser ablation, the temperature of the substrate is the most important parameter for controlled fabrication of SiNWs, which directly affects the morphology of products. In the aspect of quantity and quality of SiNWs, the two methods are also equal. The preparation process generally does not adopt metal as catalytic avoiding the pollution from metal, and the yield is amazing. The diameters of the products varied from 13 to 30 nm, and the mean value was about 20 nm. Lee and co-worker synthesized large areas of highly oriented, very long SiNWs by thermal evaporation of SiO powder [58]. In addition, different temperatures of the substrate can obtain different morphologies of silicon nanostructures. Pan et al. fabricated silicon-based nanostructures with different morphologies such as octopus-shaped, pin-shaped and wirelike on Si wafers by thermal evaporation of SiO powders at 1350 °C [68]. The shortcoming of this method is the high temperature up to 1300 °C. High-density, PSNA were fabricated on silicon substrates by the simple thermal-evaporation oxide-assisted growth (OAG) method assisted with Au catalyst in a hot filament CVD system [69]. The OAG method can produce SiNWs in large quantities and without metal contamination, but with less control in wire pattern and diameter. The metal-catalytic VLS method offers better control of diameter and patterning of SiNWs but relatively low yield of production. The modified approach offers advantages over the common metal-catalytic VLS method and the OAG method.

![Fig. (2). Steps of PSNA fabrication using nanosphere lithography and MBE. Reprinted with permission from [60]. Copyright 2005 by American Chemical Society.](image-url)
Other Bottom-Up Approaches

PVD has also been used for preparation of PSNA. Recently, Kramer and co-workers investigated self-assembled PSNA grown by PVD [70]. However, the growth of SiNWs seems to be strongly dependent on the surface state.

Solution synthesis has satisfactory chemical selectivity [71-73]. Holmes and co-workers produced SiNWs with highly crystalline cores, narrow diameter size distributions, aspect ratios greater than 1000, and tunable crystallographic orientation by supercritical fluid synthesis [74]. Although this method could produce more products, the SiNWs have a wide size distribution.

Top-Down Approaches

Recently, a relatively rapid method is popular to fabricate PSNA which arises from electroless plating on a silicon wafer through selective etching. This is in contrast with conventional electroless plating which employs surface metallizing. Researchers found that when conducting HF/AgNO₃ etching on Si, aligned SiNWs and dendrite-like silver coatings can be obtained on the surface [75]. Based on the preliminary formation mechanisms and the relationship with conventional electroless plating, the new technique is termed self-selective electroless plating [76]. Although substantial progress has been made in regard to the understanding the self-selective electroless plating on Si, there are challenges in the roadmap before the technique can be used more extensively to fabricate PSNA. As for growth mechanism, some people believe that Ag protects the silicon underneath from being etched [77-79], while some others postulate that Ag particles only catalyze etching of the Si substrate in contact with them [80, 81]. Another school of thought is that the network structure of the Ag clusters affects the formation of perpendicular SiNWs [82]. However, these proposed mechanisms are not backed up by sufficient experimental evidence and some presumptions must be made. Thus, investigation of the detailed mechanism of self-selective electroless plating on Si requires more research.

It is known that the axial crystallographic orientations of 1D SiNWs are expected to influence their electronic structure (energy gap) as well as their physical properties (electron transport) according to previous theoretical calculations. Hence, the accurately controlled fabrication of PSNA with the desirable axial crystallographic orientation using simpler and quicker ways is very desirable and of great importance to materials synthesis and future nanoscale optoelectronic devices that employ silicon. In this respect, the technique of self-selective electroless plating can produce single-crystal high-quality SiNWs with the desirable crystallographic orientation readily and controllably by selecting silicon wafers with the corresponding crystallographic orientation [48].

Besides self-selective electroless plating, an improved photolithography method was also described to produce PSNA on silicon wafers. By combining the conformal deposition and anisotropic etching process, Choi and co-workers successfully produced sub-10-nm PSNA [83]. The process started from 600 nm wide wires that composite with polysilicon. Plasma etching is used repeatedly to reduce the size and remove the superfluous composite (see Fig. (3)).

The current development of the state-of-the-art optical lithography at 193 nm wavelength is pushing the limit of 32 nm (half pitch). It is generally believed that extension of the roadmap for semiconductor industry beyond 32 nm will probably require the development of “next-generation” lithography technologies such as extreme ultraviolet lithography (EUVL) and nanoimprint lithography (NIL). The EUVL

![Fig. (3). Schematic drawing of the size reduction lithography process. Reprinted with permission from [83]. Copyright 2003 by American Chemical Society.](image-url)
is a projection optical technology that uses 13.5 nm wavelength. At this wavelength, all materials are highly absorbing, so the imaging system is composed of mirrors coated with multilayer structures designed to have high reflectivity at 13.5 nm wavelength [84].

NIL is becoming an important technique both for research and industrial purpose as it is in many respects capable of producing structures comparable to, or even smaller than, those of e-beam lithography but at considerably lower cost and with much higher throughput [52]. NIL basically consists of two steps: imprint and etching. In the imprint step, a mold/stamp is first replicated from a relief-structured master, and then pressed into a thin resist cast on the final substrate, followed by the removal of the mold. The current state-of-the-art definition in NIL using electron beams is about 5 nm. It is obvious that NIL can achieve much better resolution than EUVL. Yang et al. demonstrated the combination of NIL with Au colloids for the growth of PSNA [63]. Kamins et al. invented methods to produce arrays of catalytic nanoislands by one or more nanoimprinting steps [85]. The invention is useful for forming PSNA.

PROPERTIES AND APPLICATIONS

High Antireflection Property and Photovoltaic Application

One of the most important features of PSNA is the significant suppression of reflection over the visible-light spectral range. Compared to thin films, PSNA with moderate filling ratio have a much lower reflectance in a wide spectrum range which can be achieved without specially designed antireflection coating [86]. Si substrates using self-selective electroless plating can diminish the reflection drastically over a wide spectral bandwidth from 300 to 1000 nm [32]. The reflectance from the arrays on single crystalline Si is about 1.4% and much less in the range of 300–600 nm. It is believed that this remarkable property arise from the high density of the PSNA, because the sub-wavelength structured surface can suppress reflection over a wide spectral bandwidth and a large field of view, in addition to the introduction of a possible porosity gradient throughout the PSNA.

The optical antireflection behavior of the PSNA closely resembles that of a multi-antireflection coating and bodes well for applications to high-efficiency Si solar cells. Peng and co-workers have investigated SiNWs from the perspective of photovoltaic applications [32, 38]. However, the photovoltaic conversion efficiency is not as high as that expected of the excellent anti-reflecting properties. In order to improve the important photovoltaic parameters such as short-circuit current and open-circuit voltage, phosphorus diffusion and fabrication of contacts need to be optimized. Consequently, in spite of the potential, the efficiency of these nanowire-based photovoltaic cells prepared by self-selective electroless plating needs further improvement and investigation. Recently, a novel large-area ordered silicon nano-conical-frustum array structure, exhibiting an impressive absorbance of ~99 % (upper bound) over wavelengths 400–1100 nm with a thickness of only 5 μm, is demonstrated by using the self-powered parallel electron lithography technique that has the potential for very high lithography throughout, high resolution, and low cost. Moreover, high-efficiency (up to 10.8 %) solar cells are demonstrated using these ordered ultrathin silicon nano-conical-frustum arrays [87].

Inspired by the approach to fabricate SiNW p-n junction diode arrays [88], Cheng et al. have prepared p-poly(9, 9-diethylfluorene) (PDEF)/n-SiNW heterojunctions by spin coating p-type conductive organic polymer on as-prepared n-SiNWs fabricated by self-selective electroless plating [89]. The main advantage of such hybrid devices is the possibility of altering the composition of the organic film to effect large changes in its optical and electronic properties. In addition, the high injection current with quantum effects at nanosized junctions formed by crossing p- and n-type nanowires indicates that high performance devices can be developed by employing nanowires in the structures. Hence, the p-PDEF/n-SiNW heterostructure is expected to have high efficiency by improving the carrier injection efficiency through the nanosized junctions.

Thermal Conductivity

Recently study showed that phonon transport within crystalline silicon can be significantly altered when crystalline silicon is confined to the nanometer range. This phenomenon can be explained by various effects such as the increase in boundary scattering, the change of phonon dispersion relation and the quantization of phonon transport [90]. Molecular dynamics simulations show that the thermal conductivities of nanometer wires could be two orders of magnitude smaller than that of bulk silicon. Li and co-workers have measured thermal conductivities for intrinsic single-crystalline PSNA of different diameters (22, 37, 56, and 115 nm) shown in Fig. (4a) [10]. Compared to bulk silicon, all the SiNWs have two important features: (i) the measured thermal conductivities are about two orders of magnitude lower than that of the bulk. When the wire diameter is decreased, the corresponding thermal conductivity is reduced. This indicates that enhanced boundary scattering controls phonon transport in SiNWs; (ii) Thermal conductivities of the 37, 56, and 115 nm diameter wires reach their peak values around 210, 160, and 130 K, respectively. This is in sharp contrast to the peak of bulk Si which occurs at about 25 K. As the wire diameter is reduced, the phonon boundary scattering dominates over phonon-phonon Umklapp scattering, which decreases the thermal conductivity with an increase in temperature.

Hochbaum and co-workers found that electroless etching Si nanowires exhibit a diameter dependence of thermal conductivity similar to that of VLS-grown wires [91]. The magnitude of thermal conductivity is five- to eightfold lower for electroless etching nanowires of comparable diameters (see Fig. (4b)). Because the phonon spectrum is broad and Planck-like, thermal conductivity can be reduced by introducing scattering at additional length scales beyond the nanowire diameter. Although bulk Si is a poor thermoelectric material, by greatly reducing thermal conductivity without much affecting the Seebeck coefficient and electrical resistivity, PSNA show promise as high-performance, scalable thermoelectric materials.
Raman Spectroscopy and Field Electron Emission Properties

Raman spectroscopy has already been extensively applied for SiNWs to explain the shape and position of the Raman peak describing phonon confinement [92, 93]. Scheel et al. observed an asymmetric Raman peak in SiNWs, which is redshifted and broadened compared to the optical phonon of bulk silicon. Shifting and broadening increase with increasing laser power which has been attributed to heating [94]. Li and co-workers synthesized PSNA by self-assembling electroless nanoelectrochemistry [95]. They found the first-order Raman peak of SiNWs is at 516.2 cm\(^{-1}\) with an full-width at half-maximum (FWHM) of 14.2 cm\(^{-1}\). The phonon quantum confinement effects of the PSNA were confirmed through the downshifting, broadening and asymmetry of the first-order Raman peak. The size-dependent Raman shift was also investigated, in which Raman shift increased with the decrease of the diameter of SiNWs.

Field electron emission from the SiNWs also has been investigated by Li [8]. The turn-on field is about 12 V/μm at a current density of 0.01 mA/cm\(^2\). These highly densified PSNA are expected to have favorable applications in vacuum electronic or optoelectronic devices.

Biological and Chemical Sensors

PSNA have some remarkable characteristics such as large superficial area, excellent surface activity and sensitive in temperature, light, moisture and other environmental factors. The changing of the external environment quickly causes the changing of the surface or interface ion valence electron transport. Thus, it is possible to use the significant change of the resistance for the fabrication of nanosensors.
Gao and co-workers have reported biosensors based on PSNA which exhibit the expected surface-charge-induced resistance response upon hybridization with complementary [30]. Compared to other DNA assays, PSNA biosensor has four advantages: (i) ultrasensitive and label-free, (ii) more cost-effective than optical biosensor arrays, (iii) rapid, direct, turbid, and light absorbing-tolerant detection, (iv) portable, robust, low-cost, and easy-to-handle electrical components suitable for field tests and homecare use. Li and co-workers fabricated highly sensitive and sequence-specific DNA sensors by SiNWs with single stranded probe DNA molecules covalently immobilizing on the nanowire surfaces [28]. A change of the conductance of the SiNWs is made when the target DNA is hybridized with the probe DNA attached on the SiNW surface. For a 12-mer oligonucleotide probe, a 25 pM solution of target DNA is detected easily.

Field-Effect Transistor

SiNWs are attractive components for nanoelectronics because they can exhibit a range of device function and serve as bridging wires. VLS SiNWs FETs with high mobility and low subthreshold swings have been reported by the Lieber group [96, 97]. Schmidt et al. have presented a generic process flow to fabricate PSNA vertical surround-gate FETs [21]. One of the advantages of the fabrication is that the vertical surround-gate FET does not include any chemical or mechanical polishing step. The nanowires were grown on the substrate in stripe-shaped regions of a few hundred micrometers in width. The gate and source contacts were defined using optical lithography and lift-off techniques. In the demonstrated device, n-doped SiNWs grown epitaxial on a p-doped substrate were used as active material. The array of vertical surround-gate FETs exhibited a gate-voltage-dependent current increase of more than two orders of magnitude.

CURRENT & FUTURE DEVELOPMENTS

SiNWs are attracting much attention due to their technical compatibility with existing semiconductor technology. Usually, SiNWs are grown with random orientations and further processing is required to assemble the nanowires for specific applications. For device applications, one important challenge that needs to be overcome is obtaining precise control of the size, crystallographic orientation, location, and packing manner of the SiNWs. Although both the templated and the VLS-synthesized SiNWs can be prepared with an alternating and controllable stoichiometry along the long axis of the nanowire, these SiNWs need to be organized into the desired device setting, and that still remains a challenge. In this Review, recent advances in PSNA have been discussed. Substantial progress has been made with regard to the growth approaches for PSNA. However, there are challenges in the roadmap before integration of well aligned SiNWs into devices with existing technologies. Thus, research on PSNA is still in the beginning stage and progress is needed for more widespread applications of this technique in nanotechnology.

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CONFLICT OF INTEREST

The author declares no conflict of interest.

REFERENCES

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Recent Patents on Nanotechnology


