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Strain Stability and Carrier Mobility Enhancement in Strained Si on Relaxed SiGe-on-Insulator

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A low thermal budget process to fabricate strained Si metal-oxide-semiconductor field-effect transistors (MOSFETs) on a strain-relaxed silicon–germanium-on-insulator (SGOI) by strain engineering is described. The strain stability in the top strained Si is studied after low temperature oxidation, ion implantation, and rapid thermal annealing, and only 7–9% relaxation is observed. The Ge content distribution in a strained-silicon-on-insulator (SOI) is investigated to validate the process with a low thermal budget. Ge, reaching the strained Si/SiO_2 interface, inevitably degrades the gate oxide properties. The electron and hole mobility values in the biaxial strained-SOI are investigated and compared to those in MOSFETs fabricated in strain-relaxed SGOI and SOI substrates. Both carrier mobilities are enhanced, and the process is much simpler than using uniaxial strained Si. The relaxed-SGOI MOSFETs possess the lowest carrier mobility, and both the electron and hole mobility values in the strained-SOI MOSFETs are enhanced compared to the devices fabricated in the control samples and bulk Si. The SiGe layer in strained-SOI can lead to a larger leakage current.
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Strain engineering is one of the most technologically important methods to improve the performance of both n- and p-metal-oxide-semiconductor field-effect transistors (MOSFETs).[1-3] Process-induced stress in the transistor channels, such as uniaxial tensile stress in n-metal-oxide-semiconductor (MOS) and the compressive stress in p-MOS, works well in the sub-90 nm technology nodes. However, in the 45 nm node and beyond, adoption of biaxial tensile strain appears to be more suitable.

The strain-relaxed SiGe-on-insulator (SGOI) substrate fabricated by Ge condensation is generally regarded to be an appropriate stressor for strained Si epitaxy.[4-7] The smooth SGOI surface also bodes well for strained Si growth. During condensation when the SiGe layer is oxidized, Ge atoms are rejected from the surface oxide layer into the underlying unoxidized SiGe. Thus, the strain in the top Si can be controlled by changing the condensation time or temperature. Moreover, the strained Si layer on the relaxed-SGOI [strained-silicon-on-insulator (SOI)] is an ideal platform for partially depleted complementary metal oxide semiconductor (CMOS) due to its benefits, such as enhanced mobility and reduced junction capacitance.[8] Tezuka et al. achieved an enhanced electron mobility of up to 67% in strained-SOI n-MOSFETs.[3] However, the hole mobility enhancement and strain relaxation in the fabrication process have not been investigated in detail. Mizuno et al. developed a high performance strained-SOI CMOS device on a relaxed-SGOI. The electron and hole mobility values in the strained Si devices were observed to improve by 85 and 53%, respectively.[2] In their experiments, the buried oxide layer was produced by separation by implantation of oxygen (SIMOX), encompassing a high fluence oxygen ion implantation (4×10^{17} cm^{-2}) and postannealing at over 1300°C, thereby limiting the applications. Drake et al. investigated strain relaxation in strained Si following rapid thermal annealing (RTA) at temperatures as high as 950°C and no strain relaxation was observed.[9] Here, the temperature was relatively low, and the annealing time was only 1 s, making it difficult for other conventional fabrication processes.

In this paper, we introduce an optimized condensation technique to fabricate the strain-relaxed SGOI layer by the oxidation of a sandwiched Si/SiGe/SOI structure and subsequently by deposition of a >20 nm thick strained Si layer on the SGOI substrate. The stability of the strained Si is studied after oxidation at 780°C, implantation, and RTA at 1020°C for 30 s. Raman spectroscopy, transmission electron microscopy (TEM), energy-dispersive X-ray spectroscopy (EDS), atomic force microscopy (AFM), and electrical measurement are employed to characterize the materials.

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Experimental

Commercial (150 mm in diameter) SIMOX wafers (50 nm thick top silicon and 376 nm thick buried oxide) were used in our experiments. The SiGe and Si were deposited in an ultrahigh vacuum chemical vapor deposition (UHV-CVD) reactor at 500°C. The relaxed-SGOI substrate of the sandwiched structure of 20 nm Si/100 nm or 150 nm $Si_{0.85}Ge_{0.15}$/SOI was fabricated by dry oxidation at 1100°C. Finally, a high quality strained Si film (about 20–30 nm) was grown on the relaxed-SGOI surface after removing the surface oxide layer formed in the condensation process. Two strained Si layers were fabricated on the SGOI with different Ge concentrations (18 and 29%), and the latter one was used in our MOSFET fabrication. Cross-sectional TEM (CM200FEG system) was performed to assess the quality of the strained Si. The distribution of Ge in SiGe was determined by EDS in conjunction with TEM.

The n- and p-MOSFETs were fabricated on the strained-SOI, relaxed-SGOI, and SOI by conventional self-aligned poly-Si gate processes. To reduce Ge diffusion in the strained Si layer, dry–wet–dry oxidation was performed at 780°C for 15, 5, and 10 min, respectively. The oxide thickness in the strained-SOI was about 6 nm. The source/drain structures were formed by RTA at 1020°C for 30 s after As^+ (90 keV, 5×15 cm^{-2}) and B^+ (40 keV, 5×15 cm^{-2}) implantation with a sacrificial oxide. UV Raman spectroscopy was utilized to evaluate the strain stability during the key processes including oxidation, implantation, and RTA. The reduced penetration depth of UV Raman (325 nm emission line of a He–Cd laser) in Si considerably improved the detection of the strain localized close to the Si surface. Thus, only the Si–Si mode from the top strained Si was detected, whereas the Si–Si mode from underneath the SiGe layer or the Si substrate was not visible. The current–voltage (*I-V*) and split capacitance–voltage (*C-V*) characteristics were measured by a Keithley 4200 semiconductor parameter analyzer and an Agilent 4284 LCR meter, respectively.

Results and Discussion

TEM was used to determine the crystalline quality of the strained Si film fabricated by CVD. Figure 1 displays the cross-sectional TEM images of the strained-SOI structure and the Ge concentration profile across the layers determined by EDS. The SiGe layer is formed on the 100 nm $Si_{0.85}Ge_{0.15}$ sample. No threading dislocations can be observed, and the layer interface can be clearly delineated.

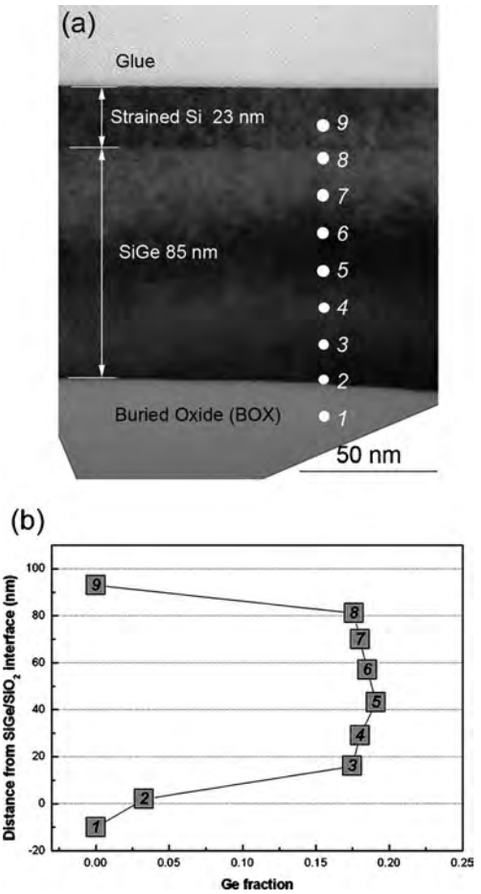

Figure 1. (a) Cross-sectional TEM image of the strained-SOI structure deposited by UHV-CVD and (b) lateral Ge concentration profile across the various layers determined by EDS.

As shown in Fig. 1b, the Ge fraction is about 0.18 ± 0.01 with good uniformity. The surface morphology of the top strained Si was also measured by AFM, and the root-mean-square roughness was calculated to be 0.9 nm from a scanned area of 10 × 10 μm.

To evaluate the strain stability, Raman spectra excited by a 325 nm source are obtained and depicted in Fig. 2. To obtain better statistics, three different locations on each sample were measured. The degree of relaxation in the strained Si after dry oxidation and implantation (with ensuing RTA) can be determined from Fig. 2a and b. The strain $\varepsilon^{\text{strained-Si}}$ in the top strained Si can be calculated from the Raman shift ($\Delta\omega_{\text{Si–Si}}^{\text{strained-Si}}$), which is defined as $\Delta\omega_{\text{Si–Si}}^{\text{strained-Si}} = b_{\text{Si–Si}}^{\text{strained-Si}} \times \varepsilon^{\text{strained-Si}}$, where $b_{\text{Si–Si}}^{\text{strained-Si}}$ equals -784 ± 4 cm^{-1}.[10] According to the Raman signal acquired from the strained Si, the tensile strain $\varepsilon^{\text{strained-Si}}$ is determined to be 0.007. This value is consistent with the EDS results in Fig. 1 in which $Si_{0.82}Ge_{0.18}$ can induce a strain of about 0.0075. In Fig. 2a, the peak corresponding to the Si–Si mode in the strained Si layer shifts from 515.3 to 515.7 cm^{-1}, indicating a relaxation of about 7%, whereas Fig. 2b illustrates that after implantation and RTA, the relaxation is about 9%. Although the observed relaxation is small, it is very encouraging for the MOSFET fabrication as most of the strain is maintained during the thermal or implantation process. After implantation and RTA, the Raman peak obtained from the strained Si in Fig. 2b is broadened compared to the sample after oxidation at 780°C in Fig. 2a. Falkovsky et al. reported that the interaction of phonons with static strain fluctuations induces a broadened Raman spectra.[11] Here, we believe that the temperature factor is more important in the relaxation process. The thermal mismatch between the strained Si and the relaxed SiGe layer is a significant contributor to the broadening of the Raman peak, which is consistent with Samavedam et al.'s results.[12]

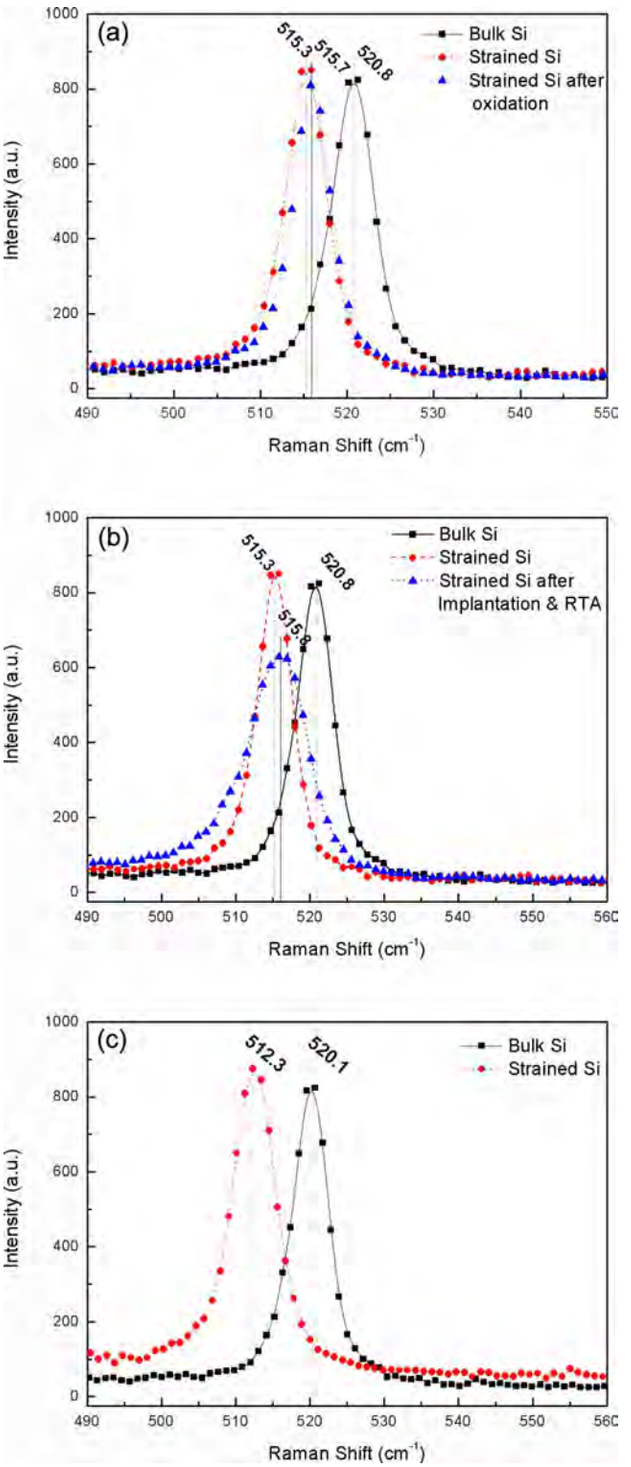

Figure 2. (Color online) Raman spectra acquired from strained-SOI samples: (a) Strained Si on relaxed $Si_{0.82}Ge_{0.18}OI$ before and after dry oxidation at 780°C for 30 min, (b) strained Si on relaxed $Si_{0.82}Ge_{0.18}OI$ before and after implantation (As^+, 90 keV, 5 × 15 cm^{-2}) and RTA at 1020°C for 30 s, and (c) strained Si on relaxed $Si_{0.71}Ge_{0.29}OI$ substrate.

To achieve a larger tensile strain in the strained Si film, the

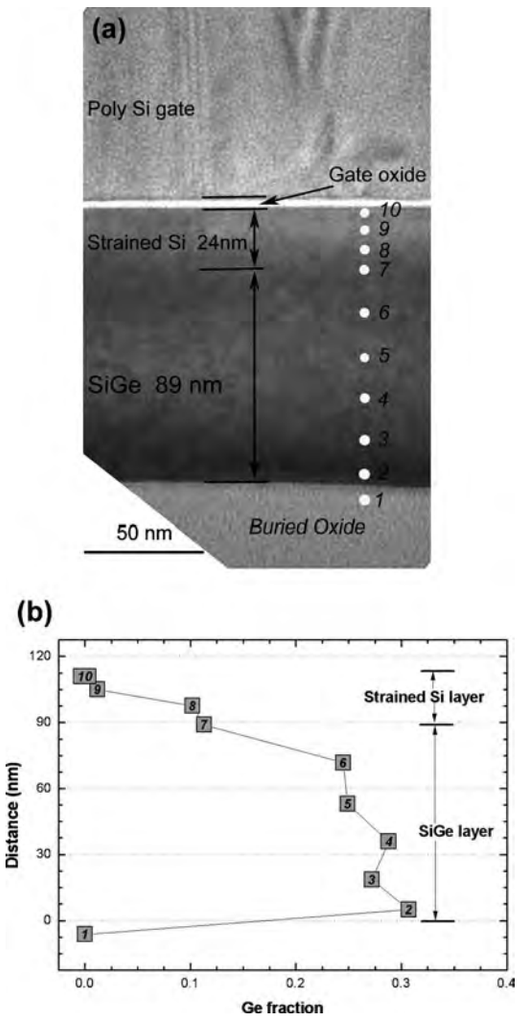

Figure 3. (a) Cross-sectional TEM image of the strained-SOI MOSFET structure (strained Si on relaxed $Si_{0.71}Ge_{0.29}OI$) with a poly-Si gate deposited by low pressure chemical vapor deposition. (b) Lateral Ge concentration profile across the channel determined by EDS showing Ge diffusion across the strained Si/SiGe interface.

relaxed-SGOI substrate with a higher Ge fraction (about 0.29 ± 0.01) was fabricated by oxidation of the 20 nm Si/150 nm $Si_{0.85}Ge_{0.15}$/SOI structure. The original tensile strain in the strained Si layer could be 0.012. Figure 2c shows the Raman shift of the Si–Si vibrational mode in the bulk Si and the strained Si with a higher tensile strain. Here, the Si–Si peak of the strained Si is located at 512.3 cm^{-1}, and so the tensile strain $\varepsilon^{\text{strained-Si}}$ is 0.01, which is also consistent with the EDS results.

Figure 3 displays the cross-sectional TEM images of the final strained-SOI MOSFET structure with a smooth gate oxide together with the Ge profile determined by EDS. After the MOSFET fabrication process, the interface between the SiGe and the strained Si layer becomes less abrupt. During the doping process, radiation-enhanced diffusion or intermixing under ion irradiation may be a reason for the disappearance of the interface. More work is performed to fathom the exact mechanism. According to the Ge distribution in Fig. 3b, Ge atoms cannot be detected in the top of the strained Si layer, but Ge diffusion (high to low concentrations) is apparent across the strained Si/SiGe interface. A low temperature oxide or high-*k* dielectric layer may mitigate such diffusion.

Figures 4 and 5 exhibit the typical drain current (I_{ds}-V_{ds}) characteristics of n- and p-MOSFETs fabricated in the three substrates:

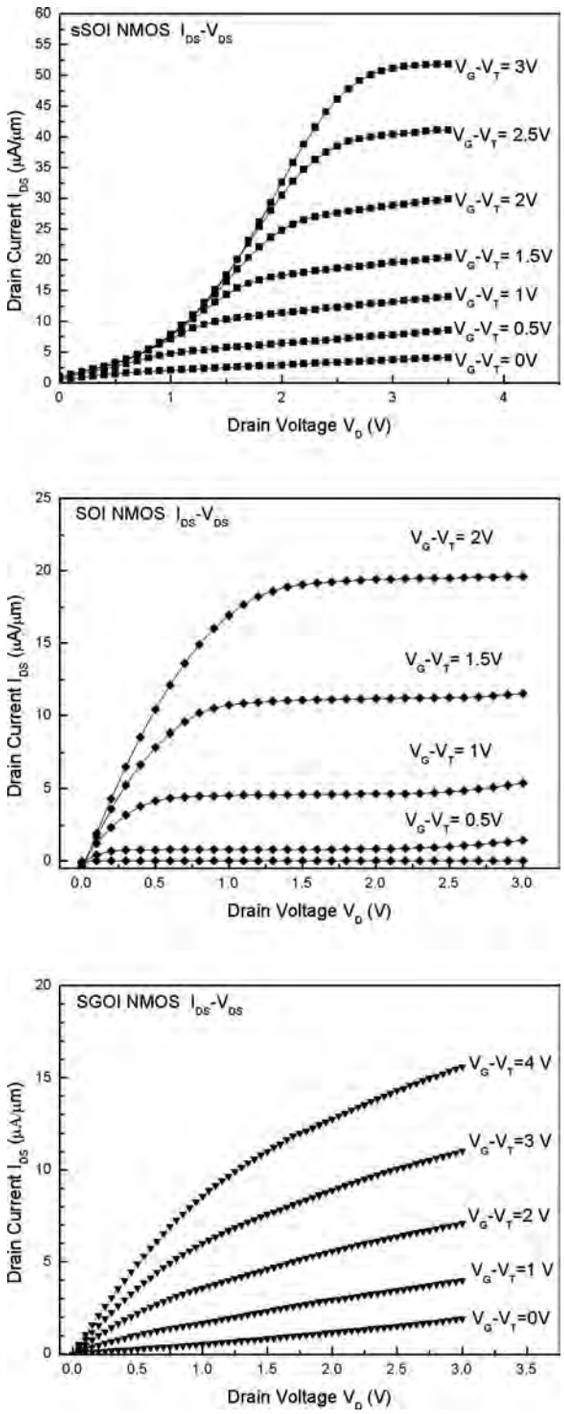

Figure 4. I_{ds}-V_{ds} characteristics at various gate overdrives (V_{gs}-V_t) obtained from the strained-SOI, control SOI, and relaxed-SGOI n-MOSFETs (gate length = 3 μm).

strained-SOI, control SOI, and strain-relaxed SGOI. The gate length in the test devices is 3 μm. Drain current enhancements of 47 and 59% are observed from the strained-SOI n- and p-MOSFETs relative to the control SOI samples. The improvement can be attributed to carrier mobility enhancement compared to that in ultrathin SOI.[13,14] Figure 6 shows the effective electron and hole mobility values as a function of the inversion charge density (Q_{inv}) determined from the I_{ds}-V_{gs} and inversion *C*-*V* data[15] using $\mu_{eff} = LI_{ds}/WQ_{inv}V_{ds}$. The

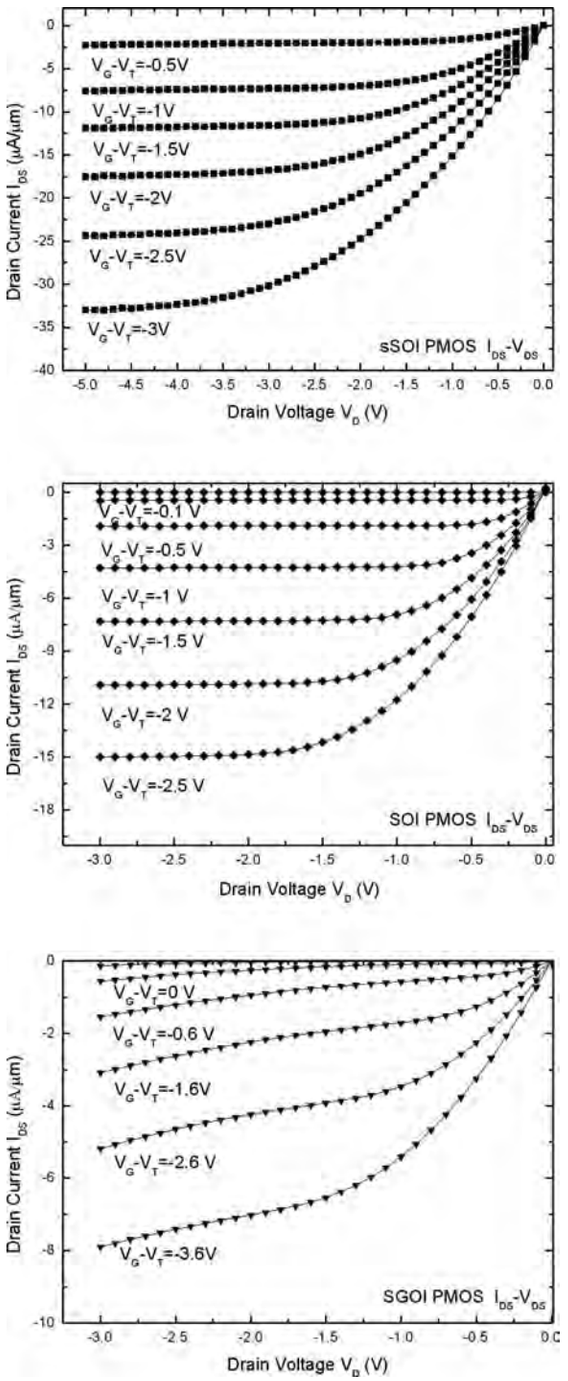

Figure 5. I_{ds}-V_{ds} characteristics at various gate overdrives (V_{gs}-V_t) obtained from the strained-SOI, control SOI, and relaxed-SGOI p-MOSFETs (gate length = 3 μm).

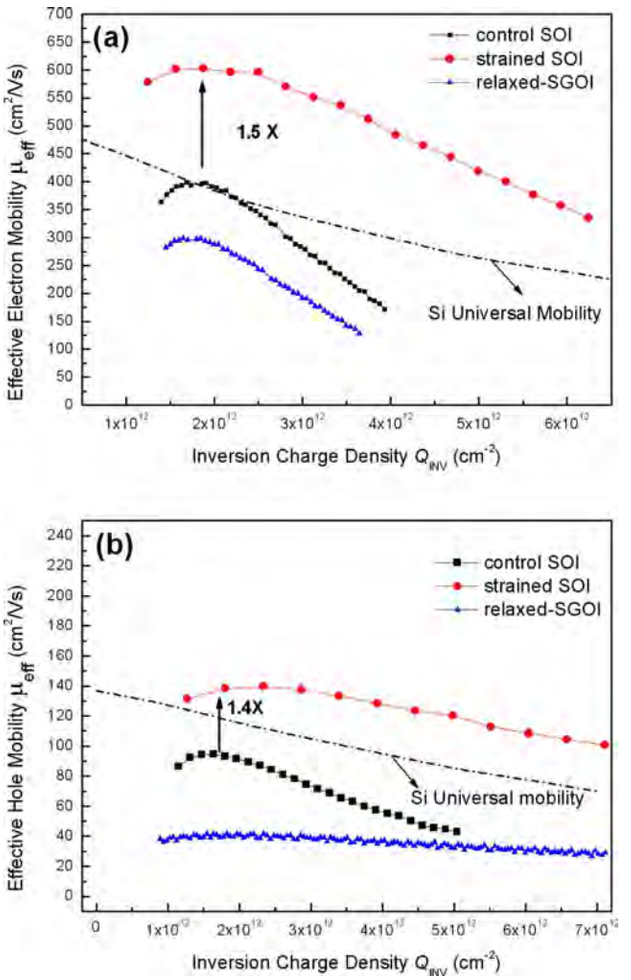

Figure 6. (Color online) Effective electron and hole values calculated from the I_{ds}-V_{gs} and inversion C-V data as a function of inversion charge density (Q_{inv}) from the inversion C-V and I_{ds}-V_{gs} characteristics. The Ge content in the strained Si and SGOI is 0.29. The universal curve for electrons and holes in Si is also shown in Ref. 12.

universal curve for electrons and holes in silicon is also shown as a reference[16] with Q_{inv} taken to be $C_{ox}(V_{gs} - V_{th})$. Because all the devices are fabricated and processed at the same time, possible errors in the approximations of Q_{inv} do not impact the comparison of the mobility characteristics. As shown in Fig. 6, the electron and hole mobility values determined from the strained-SOI MOSFETs are respectively larger by factors of 1.5 and 1.4 relative to the control SOI MOSFETs. Relatively low carrier mobilities in both devices at a low E_{eff} can be observed from Fig. 6. The relaxed-SGOI samples show the lowest carrier mobility values as well as the obvious threshold voltage shift. This low channel mobility can be ascribed to the defects present in the SGOI obtained by the Ge condensation technique. Using an enhanced secco etching technique, the defects are quantitatively evaluated. The obtained etch pit density value is about 10^6 cm^{-2}. The presence of several interfacial states may also be a reason.[17] In spite of the encouraging results, the off-leakage current is relatively large in the strained-SOI n- or p-MOSFETs. It is probably due to the structural defects near the interface between the strained Si and SiGe layers,[18] and more work is being performed to improve the process and device quality.

Conclusion

We have produced and compared n- and p-MOSFETs in biaxially strained-SOI, conventional SOI, and relaxed-SGOI. The strained-SOI substrates produced from a conventional SOI were fabricated by Ge condensation in conjunction with standard Si processes without wafer bonding and surface polishing. The effective electron/hole mobility values in the strained-SOI MOSFETs are significantly higher than those in the control SOI and relaxed-SGOI substrates. UV Raman analysis confirms that the strain in the strained-SOI is retained after oxidation, implantation, and RTA. Ge diffusion is suppressed by the low temperature process. The interface between the

strained Si and the relaxed SiGe vanishes after the implantation and the thermal process. Thus, strained-SOI without the SiGe layer is more preferred in MOSFET fabrication.

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