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B3.13 15:15 CMOS Shallow Trench Isolation x-Stress Effect on Channel Width
Philip Beow Yew Tan[1,2], Albert Victor Kordesch[1], Othman Sidek[2]
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Coffee Break (15:30-15:45)

B3.7 15:45 Fundamentals and Applications of Selenium-Passivated Si(100) Surface (invited)
M. Tao
University of Texas at Arlington, USA

B3.3 16:15 Fabrication of Novel Silicon-on-Insulator Substrates Using Plasma-Based Technology (invited)
Paul K Chu
City University of Hong Kong, Hong Kong, China

B2.19 16:45 La-based oxides for High-k Gate Dielectric Application (invited)
Parhat Ahmet, Kuniyuki Kakushima, Kazuo Tsutsui, Nobuyuki Sugii, Takeo Hattori, Hiroshi Iwai
Tokyo Institute of Technology, Japan

B2.15 17:15 Work Function Tunability by Incorporating Lanthanum and Aluminum into Refractory Metal Nitrides and a Feasible Integration Process
Xin Peng Wang[1,2], Ming-Fu Li[1,2], H. Y. Yu[3], C. Ren[1,2], W. Y. Loh[2], C. X. Zhu[1], Albert Chin[4], A. D. Trigg[2], Y. C. Yeo[1], S. Biesemans[3], Patrick Lo[2], D. L. Kwong[2]
[1]National University of Singapore, Singapore; [2]Institute of Microelectronics, Singapore; [3]IMEC, Belgiuml [4]National Chiao-Tung University, Taiwan, China

B2.16 17:30 Higher-*k* LaYOx Films with Strong Moisture-Robustness
Yi Zhao, Koji Kita, Kentaro Kyuno, Akira Toriumi

Fabrication of Novel Silicon-on-Insulator Substrates Using Plasma-Based Technology

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Abstract

Plasma-based nanotechnologies benefit the development of deep-sub-micrometer microelectronic devices. Recent works conducted in our laboratory pertaining to the production of novel silicon-on-insulator (SOI) materials to reduce the self-heating effects and the use of plasma hydrogenation to conduct ion-cutting are described in this invited paper.

1. Introduction

Development of materials for deep-sub-micrometer microelectronic devices and novel biomaterials has benefited from plasma-based nanotechnologies. As device dimensions shrink, conventional bulk silicon wafers have deficiencies and thin silicon-on-insulator materials are especially suitable for microelectronic devices such as fully-depleted metal-oxide semiconductor field effect transistors (MOSFET). In the development of novel biomaterials, plasma-based nanotechnologies offer the unique advantage that the surface properties and biocompatibility can be enhanced selectively while the favorable bulk characteristics of the materials remain unchanged. For instance, mechanically sturdy materials with good wear and corrosion resistance can be modified to improve the surface bioactivity in biomedical applications. Existing materials can thus be used and needs for new classes of materials may be obviated thereby shortening the time to develop novel and better biomedical implants. Recent works conducted in our laboratory pertaining to the production of novel silicon-on-insulator (SOI) materials to reduce the self-heating effects and improvement of surface bioactivity and properties of biomaterials are described here.

2. Novel SOI Structures

As the dimensions of metal oxide semiconductor field effect transistors (MOSFET) reach the nano regime, bulk silicon has some intrinsic deficiencies. Silicon-on-insulator (SOI) MOSFET is expected to replace conventional bulk silicon substrates in many microelectronic devices because it possesses many advantages such as the reduction of parasitic capacitance, excellent sub-threshold slope, elimination of latch up, and resistance to radiation [1]. However, wider applications of SOI in ULSI are hampered by the self-heating effects caused by the poor thermal conductivity of the buried silicon dioxide layer [2]. We have recently explored alternative buried insulators with better thermal conductivity and successfully fabricated SOI structures using aluminum nitride or diamond-like carbon as the substitute for the buried silicon dioxide layer [2]. Fig. 1 shows the TEM micrograph of the SOD (silicon-on-diamond) structure showing successful formation of the SOD structure.

Fig. 2 shows the electrical breakdown fields of the SOD samples as a function of annealing temperatures. The breakdown field of the as-deposited DLC film is 4.2 MV/cm which compares reasonably well with previously reported results. When the samples are annealed in the furnace at temperatures under 900°C, the breakdown fields do not change. When the annealing temperature reaches 900°C, the breakdown field began to decrease, but the changes were not obvious. However, when the temperature is increased to 1000°C, the breakdown field diminishes significantly. It can be inferred that graphitization of our materials does not become significant until the annealing temperature reaches 1000°C and our Raman results (not shown here) are consistent with the electrical measurements. The RTA

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results (open circles in Fig. 2) indicate that after RTA at 900°C or 1000°C, no appreciable graphitization can be detected from our electrical data. Based on our results, the DLC synthesized using the special PIII&D process can withstand furnace annealing and RTA up to 900°C, making it compatible with TFT and even conventional CMOS processing.

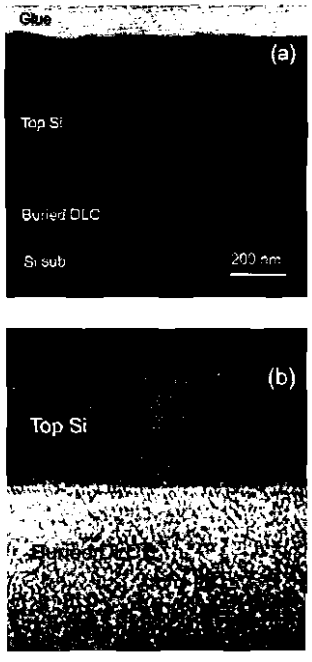

Fig. 1: (a) TEM micrograph of the SOD structure formed using direct wafer bonding and hydrogen-induced layer transfer. (b) HRTEM micrograph of the interfacial region between the top Si layer and buried DLC layer, indicating a defect-free and single crystal Si layer as well as an abrupt bonded interface.

The high resistance against graphitization has been investigated and the presence of hydrogen in the DLC layer retards this deleterious process up to about 900°C [4]. We compare the thermal stability of exposed and buried DLC films using Raman spectroscopy and x-ray photoelectron spectroscopy (XPS). Our Raman analysis indicates that the obvious separation of the D and G peaks indicative of nano-crystalline graphite emerges at 500°C in the exposed DLC film. In contrast, the separation appears in the buried DLC film only at annealing temperatures above 800°C. Analysis of the XPS C_{1s} core level spectra shows that the (sp^3+C-H) carbon content of the unprotected DLC film decreases rapidly between 300-700°C indicating the rapid transformation of sp^3-bonded carbon to sp^2-bonded carbon combined with hydrogen evolution. In comparison, the decrease in the (sp^3+C-H) carbon content in the buried DLC film is slower below 800°C. Elastic recoil detection (ERD) results show that this superior thermal stability is due to the slower hydrogen out-diffusion from the buried DLC film thereby impeding the graphitization process. Our results thus show that the SiO_2 overlayer retards the graphitization process during annealing by shifting the chemical equilibrium.

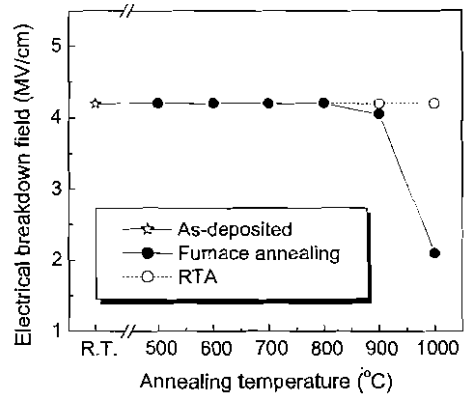

Fig. 2: Influence of annealing temperature on electrical breakdown fields for the DLC films. Filled and open circles represent results from furnace annealing and RTA in nitrogen ambient. The star is the as-deposited sample.

3. Plasma Hydrogenation

We have also recently explored the possibility of using low-energy plasma hydrogenation instead of hydrogen implantation to perform ion-cutting and layer transfer with regard to SOI fabrication [5, 6]. Boron ion implantation is used to introduce H-trapping centers into Si wafers to illustrate the idea. Instead of the widely recognized interactions between boron and hydrogen atoms, our results show that lattice damage, i.e., dangling bonds, traps H atoms and can lead to surface blistering during hydrogenation or upon post-annealing at higher temperature. The B-implantation and subseqnent processes control the uniformity of H-trapping and the trap depths. While the trap centers are introduced by B-implantation in

this study, there are many other means to do the same without implantation. Using this technology, we have successfully fabricated SOI structure using this novel technology, as shown in Fig. 3 [7].

Our process starts with p-type 1-35 Ω-cm <111> Si wafers. A dose of 5 x10^{15} cm^{-2} B^+ is implanted into the Si substrates at 170kV, followed by boron activation at 900°C in N_2 for 20 minutes. Plasma hydrogenation is conducted at 280°C in a plasma immersion ion implanter (PIII) with a radio frequency (RF) plasma source for 10 minutes [8]. These conditions are selected to introduce sufficient hydrogen atoms into the substrates but without causing surface blistering to arise directly after plasma hydrogenation. After Ar plasma activation of the sample surface, the hydrogenated sample is bonded to a Si handle wafer with an oxide top layer. Finally, the bonded structure is thermally annealed at 400°C to induce Si layer splitting and transfer, yielding the SOI structure exhibited in Fig. 3.

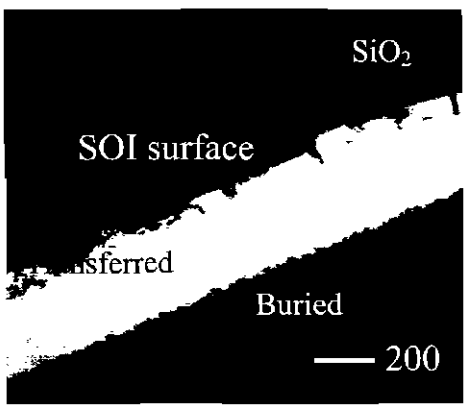

Fig. 3: Cross-section transmission electron micrographs obtained from the final SOI sample fabricated by plasma hydrogenation combined with wafer bonding.

The hydrogen distribution in the final SOI sample is examined by ERD (not shown here). Within the detection limits of ERD, no noticeable H presence is seen in the bulk of the transferred Si layer, other than a surface H concentration peak. Fig. 4 shows RBS channeling results from the final SOI sample. The average value of the channeling minimum yield (χ_{min}) in the entire as-transferred Si layer is ~8% which can be further improved by annealing. These results indicate the capability of the plasma hydrogenation process for fabrication of high-quality Si transferred layers, with implanted B damage as trapping centers.

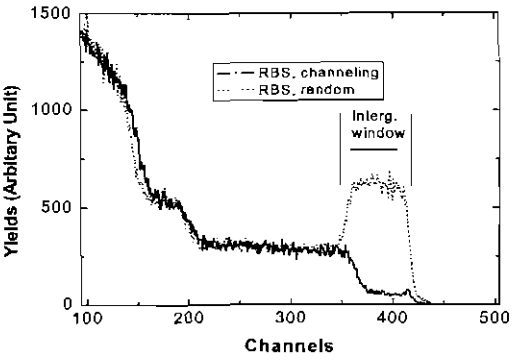

Fig. 4: RBS random and channeling spectrum from the final SOI sample. RBS analyses were performed using a 2.0 MeV He analyzing beam.

As a result of our success to use plasma hydrogenation to fabricate SOI, we have further studied the feasibility of using plasma hydrogenation for $Si_{1-x}Ge_x$ layer transfer, which is critical for the fabrication of SiGe-on-insulator (SGOI), strained Si on insulator (SSOI) and related materials. The purpose of this work is to investigate an alternative approach that replaces the hydrogen ion implantation step with plasma hydrogenation in order to avoid the shortcomings caused by hydrogen implantation. The effects of He-induced strain relaxation on hydrogen trapping are also examined.

SiGe/Si heterostructures consisting of a 210 nm thick $Si_{0.79}Ge_{0.21}$ epitaxial layer on <100> p-Si substrate with a resistivity of 1-10 Ω-cm are fabricated by chemical vapor deposition (CVD). A portion of the as-grown sample is implanted with 1.5x10^{16} cm^{-2} He^+ at 45 kV and then annealed at 850°C for 10 minutes in argon to relax the as-grown strained SiGe/Si heterostructure. Hydrogenation is conducted and the sample holder is subjected to a negative bias of several hundred volts and heated to 320~380°C for 1.5 hours.

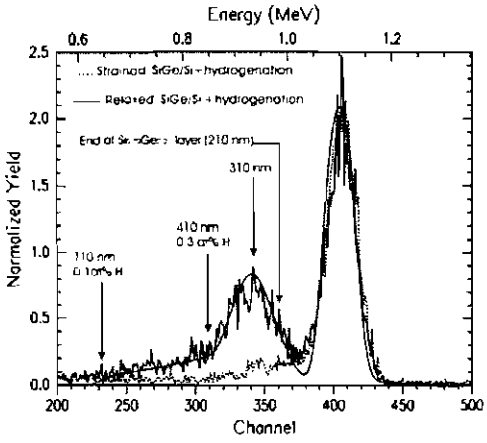

Fig. 5: He^+ Elastic recoil detection spectra acquired from hydrogenated $Si_{0.79}Gc_{0.21}/Si$ heterostructures: (a) CVD as-grown; (b) after He^+ implantation and post-annealing.

After hydrogenation, both samples with and without He-induced relaxation show surface bubbles. The ERD spectra in Fig. 5 indicate different H distribntions in the hydrogenated samples with and without Hc implantation. A small near-surface hydrogen peak is observed in both hydrogenated samples. The peak position matches the expected implantation depth for few-hundred volts hydrogen coming into the surface of the wafer during hydrogenation. Little or no notable hydrogen content and accumulation can be detected within the bulk SiGe sample without He implantation. However, in the He relaxed and hydrogcnated sample, H atoms are trapped at a specific depth below the sample surface, resulting in a significant H peak deep in the substrate.

4. Conclusion

We have demonstrated the use of plasma-based technology to fabricate novel SOI substrates with less self-heating effects such as silicon-on-diamond. We have also shown the feasibility of using plasma hydrogcnation of Si wafers for layer transfer to form SOI structures. Boron ion implantation is used as an illustrative example to create H trapping sites within a Si substrate. A uniform Si layer, relatively free of defects, is successfully transferred onto a handle wafer, and thus a SOI structure is obtained. Besides, the feasibility of using plasma hydrogenation for relaxed SiGe layer transfer has been investigated. It is found that relaxation of the as-grown strained SiGe layer is necessary to enable trapping of H atoms deep in the substrate.

Acknowledgements

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