IWJT-2006

Extended Abstracts of the Sixth International Workshop on Junction Technology

May.15-16, 2006, Shanghai, China

Editors: Yu-Long Jiang, Guo-Ping Ru, Xin-Ping Qu, and Bing-Zong Li

IEEE Press

IEEE Catalog Number: 06EX1256C

ISBN: 1-4244-0048-1

Thermal Stability and Electrical Properties of High-*k* Gate Dielectric Materials

A. P. Huang, and Paul K. Chu*

Department of Physics and Materials Science, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China

* Corresponding author: E-mail address: paul.chu@cityu.edu.hk; Tel: [852]-27887724; Fax: [852]-27889549

Abstract

The use of SiO_2 thin films as the gate dielectric is quickly reaching a limitation due to the rapid increase in tunneling current and worsened device reliability. A logical alternative is to use a gate insulator with a higher relative dielectric constant (high-*k*) than silicon dioxide (3.9), thereby spurring tremendous research activities to produce better high-*k* gate dielectric materials. In this paper, the recent progress made in our laboratory on the high-*k* materials is described. The various means to improve the thermal stability of high-*k* materials like Ta_2O_5, ZrO_2, and HfO_2 deposited on Si and their electrical properties will be discussed. The characteristics of Al_2O_3 gate dielectrics on fully-depleted SiGe-on-insulator (SGOI) will also be described.

1. Introduction

The success of the semiconductor industry relies on the continuous improvement of integrated circuit performance, which is achieved by reducing the dimensions of the key components in the circuits: the MOSFETs (Metal-oxide-semiconductor field effect transistors). One of the key elements that allow successful scaling of silicon-based MOSFETs is certainly the excellent material and electrical properties of the gate dielectric used so far in these devices. The SiO_2 gate dielectric layers have been made as thin as 1.5 nm. However, further scaling of the SiO_2 gate layer thickness is problematic which can result in a large increase of the leakage current and jeopardize device reliability [1]. Therefore, a promising alternative way is to use an insulator with a higher relative dielectric constant (high-*k*) than SiO_2 as the gate layer to reduce the leakage current and improve the reliability of the devices. Recently, there are worldwide research efforts on the investigation of high-*k* gate dielectrics for the application in advanced complementary metal-oxide-semiconductor (CMOS) technologies. The 2005 edition of the *International Technology Roadmap for Semiconductors* (ITRs) anticipates the use of high-*k* gate dielectrics in production as early as 2007 [2]. Nevertheless, many factors that negatively impact the application of high-*k* materials are found. Among them, the thermal stability of high-*k* gate dielectrics is one of the most important issues. According to the 2001 ITRs roadmap, ion implanted dopants can be electrically activated by post-annealing between 450°C and 800°C to realize ultra shallow junctions for source drain extensions to satisfy the device junction roadmap requirements for the 65 nm node and beyond. Unfortunately, the most promising high-*k* materials such as ZrO_2 and HfO_2 usually crystallize at temperatures below 500°C, and Ta_2O_5 is thermally unstable in the interface between the films and Si substrate. It seriously limits the applications of high-*k* materials in ultra large-scale integrated (ULSI) circuits. Consequently, it is necessary to control the thermal stability of high-*k* materials and make them more compatible with semiconductor processing and suitable as gate dielectrics.

1-4244-0047-3/06/$20.00 ©2006 IEEE.

Recently we have conducted extensive research to control the thermal stability and interfacial properties of high-*k* materials like Ta_2O_5, ZrO_2, and HfO_2 on Si by different methods and the electrical properties have also been studied. The relative characteristics of Al_2O_3 gate dielectrics on fully-depleted SiGe on insulator (SGOI) have been also investigated.

2. Interfacial and dielectric properties of sputtered Ta_2O_5 thin films by substrate biasing

In our work, Ta_2O_5 thin films were prepared by magnetron sputtering system under substrate bias assistance and the elemental composition of thin films was characterized by RBS [3]. According to the deconvoluted RBS data, an interfacial layer with graded composition is clearly shown in Fig. 1. Comparing Figs. 1(a), (b), (c), and (d), an interesting phenomenon can be observed. The thickness of the interfacial layer is almost independent of the substrate bias increase perhaps because the formation of the interface layer is mainly decided by the deposition

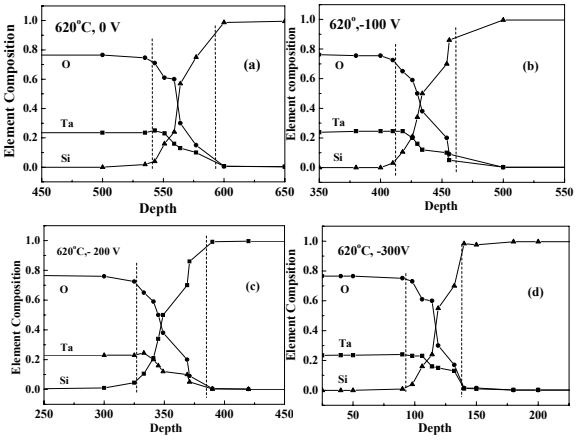

Fig. 1 Elemental depth profiles derived from the RBS data for Ta_2O_5 thin films deposited using different substrates biases

temperature, which has been confirmed by Ono *et al.* [4]. Thus, it can be deduced that the substrate bias does not affect the deposition temperature apparently but it aids to increase the nucleation density in the thin films. The ratio of tantalum to oxygen at the interface between the Ta_2O_5 and Si is different from that of the bulk film and it could influence the dielectric properties. This may be due to more diffusion of Ta into the substrate relative to that of oxygen under negative biasing conditions.

The corresponding dielectric properties of the as-deposited Al/Ta_2O_5/Si MOS structure at different substrate biases from 0 V to -200 V are shown in Fig.2. As the substrate bias increases, the capacitance value is enhanced, which corresponds to the improvement of the ability to save electrical charges in the Al/Ta_2O_5/Si MOS structure. It also means a larger permittivity as shown in Fig. 2 (d) which further indicates that the use of a suitable substrate bias can enhance the dielectric constant of the as-deposited Ta_2O_5 films. The enhancement is believed to be due to the improved crystallinity and orientation of the thin film as revealed by our XRD & FTIR results and is consistent with observations made in other studies [5]. The flatband in the *C-V* curves shifts towards the negative voltage direction as the substrate bias increases. Furthermore, the *C-V* hysteresis loop widens as the substrate bias increases and it is probably related to the larger number of slow trapping sites.

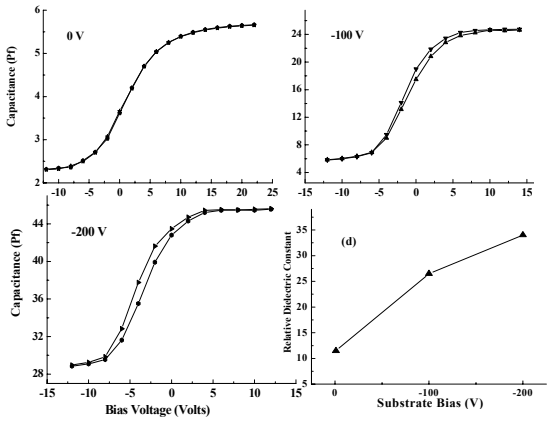

Fig.2 Forward-and-reverse *C-V* curve of Ta_2O_5 prepared at 620°C under different substrate biases and the dielectric constant of Ta_2O_5 thin films as a function of the substrate bias

According to the counterclockwise hysteresis behavior in the *C-V* curves in Fig. 2, the density of the defect states can be deduced, which is caused by the

trapping of positive charges in the oxide defect states when the MOS capacitor is stressed. The density of the slow trapping sites can be calculated and the value extracted from Fig. 2(c) for the as-deposited Ta_2O_5 is similar to that reported by Pignolet *et al* [6].

The forward-and-reverse *J-V* curves of the Al/Ta_2O_5/Si structure under different substrate biasing conditions have also been characterized and the results indicate that the leakage current density of the thin films obviously decreases as the substrate bias increases. It further indicates that by applying the proper substrate bias during magnetron sputtering, Ta_2O_5 thin films with excellent interfacial and dielectric characteristics can be obtained at low substrate temperature.

3. Thermal stability and dielectric properties of ZrO_2 thin films by plasma nitridation

In our experiments, plasma nitridation in conjunction with cathodic arc deposition was used to improve the thermal stability and dielectric characteristics of ZrO_2 thin films fabricated on Si [7]. FTIR spectra of ZrO_2 thin films on Si (100) deposited at 450°C using various gas ratios are shown in Fig.3. The thin film prepared with pure oxygen exhibits strong absorption peaks near 580, 510 and 420 cm^{-1} corresponding to the Zr-O vibrational modes. Furthermore, the weak absorption bands at around 720 cm^{-1} of Zr-O-Si and 800 & 1080 cm^{-1} of the Si-O vibration mode can be observed implying the formation of a small amount of SiO_x and $ZrSiO_x$ at the interface. In contrast, the Si-O absorption peaks can hardly be observed in the samples prepared by plasma nitridation and the intensity of the Zr-O-Si absorption peaks diminishes significantly indicating that with the addition of nitrogen, the interfacial structure of the ZrO_2/Si structure has been improved.

The HRTEM images further confirm that the ZrO_2 thin film prepared using pure oxygen has a polycrystalline phase whereas the nitridated sample is almost amorphous as shown in Figs. 4(a) and (b). Moreover, the interfacial layers in the two ZrO_2

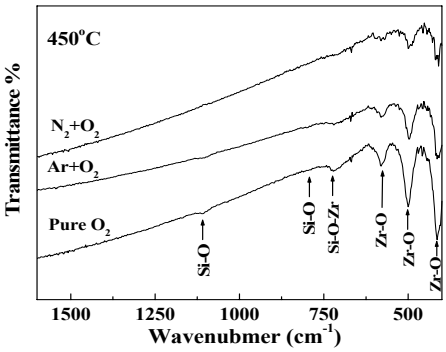

Fig.3 FTIR spectra of ZrO_2 thin films prepared at 450 °C using different working gases

samples are obviously different. The former sample shows a 2 nm thick interfacial layer while no visible interlayer can be observed in the nitridated sample, which is consistent with the FTIR results. The above results suggest that by using plasma nitridation, the growth of an interfacial layer with low permittivity can be suppressed. It is believed that plasma nitridation not only impedes crystallization and improves the thermal stability but also effectively blocks oxygen diffusion through the grain boundaries subsequently mitigating the formation of the low-*k* interfacial layer, thereby boding well for the dielectric properties of the thin films.

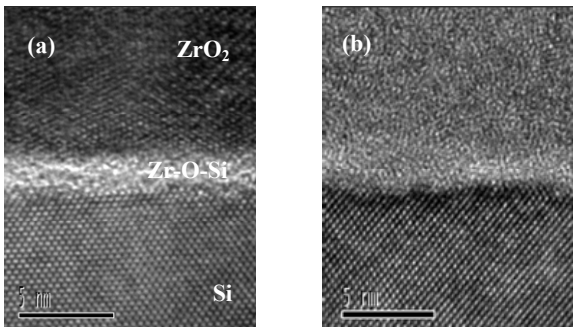

Fig.4 HR-TEM images of ZrO_2 thin films prepared at 450 °C under (a) pure oxygen and (b) oxygen mixed with nitrogen

The *C-V* characteristics of the Au/ZrO_2/Si MOS capacitors are shown in Fig. 5 and the inset in Fig. 5 indicates the corresponding *J-V* curve. With the

addition of nitrogen and argon, the accumulation capacitance value in the *C-V* curves is enhanced, which corresponds to the improvement in the ability to store electrical charges in the Au/ZrO_2/Si MOS structure. With the introduction of nitrogen, a negligible flat-band voltage shift can be observed. It is well known that the flat-band voltage shift can arise from many factors such as trapped charges at the

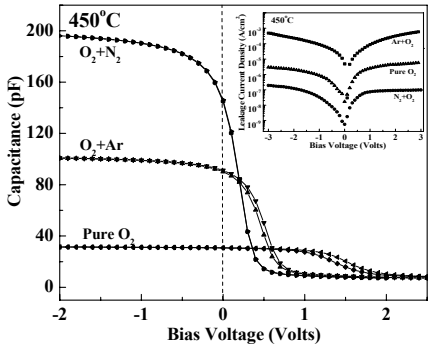

Fig.5 Forward-and-reverse *C-V* curves of Au/ZrO_2/Si MOS capacitors prepared at 450°C under different working gas ratios measured at a frequency of 1 MHz (the leakage current density as a function of voltage is shown in the insert plot)

interface and fixed charges in the oxide. Our results suggest that good interfacial properties between the nitridated ZrO_2 thin film and Si substrate can be obtained by addition of nitrogen. Moreover, the corresponding leakage current density is also significantly reduced with nitrogen incorporation. It can thus be concluded that by using plasma nitridation, the thermal stability and dielectric properties of ZrO_2/Si can be improved.

4. Control of interfacial silicate between HfO_2 and Si by high concentration ozone

In our study, HfO_2 samples were prepared by oxidation of evaporated Hf metal films on silicon substrate in high concentration (3%) ozone at low temperature [8]. The interfacial silicate layer between HfO_2 and Si substrate was controlled by introducing high concentration ozone for oxidation. Fig. 6 shows the XPS spectra of HfO_2 oxidized by ozone (denoted as ozone HfO_2 for convenience) compared to HfO_2 oxidized in oxygen (denoted as oxygen HfO_2) and as-deposited Hf metal. Prior to the analyses, about 1 nm of the surface materials was cleaned by 4 keV Ar ion bombardment. It can be seen that the Hf 4*f* core-level spectrum of ozone HfO_2 only has a Hf $4f_{7/2}$ peak at a binding energy of 17.6 eV which corresponds to the Hf-O bond in bulk HfO_2, whereas for oxygen HfO_2, two noticeable but small shoulders (indicated by arrows) at the lower binding energy side of the main peak are observed in Fig. 6 (b), which can be attributed to the Hf-Si bond due to oxygen deficient oxidation and formation of Hf-silicide. In contrast, a strong peak at 14.2 eV appears in the Hf 4*f* core-level spectrum of the as-deposit Hf metal, as shown in Fig. 6(a), which corresponds to the strong Si-Hf bond in pure Hf metal. Furthermore, a shoulder at the binding energy of 17.4 eV is also detected that is attributed to the Hf-O bond in HfO_2 or $(HfO_2)_x(SiO_2)_{1-x}$. These results from partial oxidation of the as-deposit Hf metal are observed after removal from the vacuum chamber and exposure to air. As for the Si 2*p* core-level spectra of all the samples, the main peak appears at 99.3 eV which is the binding energy of bulk Si. Only oxygen HfO_2 shows a shoulder at about 102.2 eV in the Si 2*p* spectra. This implies a more silicate-like nature at the interface between HfO_2 and H-terminated Si substrate. No increment of oxygen concentration with respect to hafnium concentration in the samples can be detected from the RBS data, in comparison to the ozone HfO_2 with oxygen HfO_2. This clearly indicates that the introduction of ozone can significantly improve the bonding nature between hafnium and oxygen.

The cross-sectional HRTEM images of both the oxygen and ozone oxidized HfO_2 samples are shown in Fig. 7. Oxygen HfO_2 in Fig. 7 (a) has a high interface roughness compared to that prepared by ozone. An interfacial region about 1.2 nm thick appears which well agrees with the results of the XPS

Si 2*p* spectra. In contrast, the ozone oxidized sample

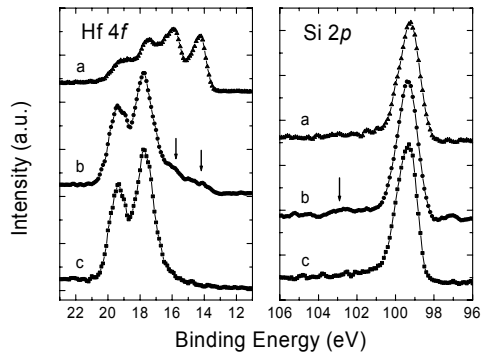

Fig.6 XPS spectra of Hf 4f and Si 2p core-levels of (a) as-deposit Hf metal, (b) oxygen HfO_2, and (c) ozone HfO_2

in Fig 7 (b) shows a sharp interface between the HfO_2 and Si substrate and no noticeable interfacial layer can be observed. This is considered to be due to the reduction of interfacial Si displacement during ozone

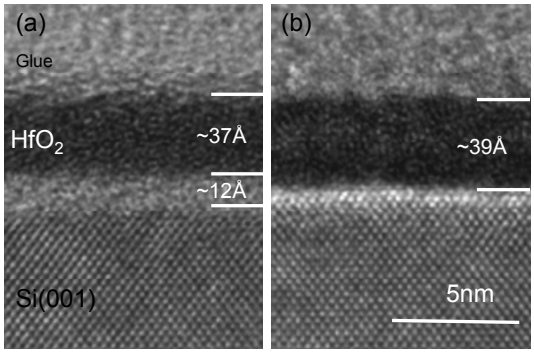

Fig.7 Cross-sectional HRTEM micrographs of (a) oxygen HfO_2, and (b) ozone HfO_2

oxidation and the layer-by-layer growth mode being predominant to form the homogenous hafnium oxides. Furthermore, the ozone HfO_2 shows excellent *C–V* characteristics, where the measured *C–V* hysteresis is negligible. This again demonstrates that ozone oxidation after Hf deposition is beneficial to improving the interface properties and reducing the charge trapping centers, in comparison to the HfO_2 sample oxidized in pure oxygen.

5. Interfacial and electrical characteristics of Al_2O_3 gate dielectric on fully-Depleted SiGe-on-Insulator

Al_2O_3 was deposited on the SiGe channel layer by electron beam evaporation using a high purity sintered powder target at room temperature and pressure of 10^{-6}~10^{-7} Pa [9]. Post-annealing was conducted under N_2 at 800°C for 30 minutes to investigate the interfacial reactions and structural characteristics of the films. Figs. 8 (a) and 8 (b) depict the cross-sectional HRTEM image of the annealed high-*k* gate dielectric on the fully-Depleted SiGe-on-Insulator (FD SGOI) substrate. In Fig. 8 (a), the Al_2O_3 gate dielectric and an interfacial layer (IL) on the FD SGOI substrate are clearly shown and the two interfaces are atomically flat. Fig. 8 (b) shows that the layer consists of a top amorphous Al_2O_3 film with a thickness of ~9.4 nm, an amorphous IL with a thickness of ~2.3 nm, and a strained SiGe channel with a thickness of ~26.7 nm. The clear lattice image without micro-twins or defects indicates that a high-quality SGOI substrate has been fabricated using Ge oxidation/condensation. Since the IL between the Al_2O_3 and FD SGOI is an integral part of the gate dielectric, the properties of this layer are investigated along with those of the Al_2O_3 film by HRXPS.

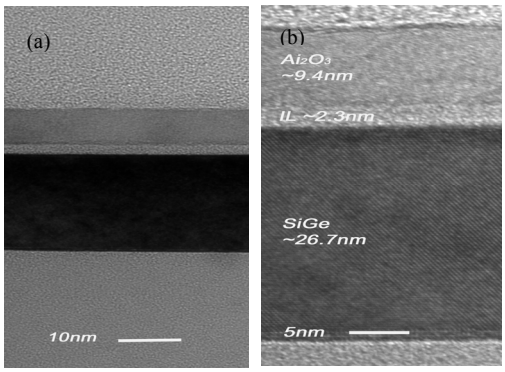

Fig.8 Cross-sectional HRTEM micrograph of annealed Al_2O_3 high-k gate dielectric fabricated on FD SGOI substrate

The electrical properties of the gate dielectric of Al_2O_3/IL/SGOI structure using an Al electrode are shown in Fig. 9 and the typical high-frequency (1 MHz) capacitance-voltage (*C-V*) characteristics of the as-deposited and annealed (800°C, 30 min) gate dielectric. In Fig. 9 (a), the hysteresis loop in the counterclockwise direction with a flat band voltage

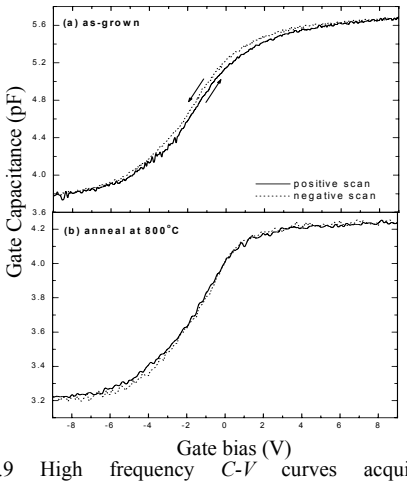

Fig.9 High frequency *C-V* curves acquired from the $Al/Al_2O_3/IL/SGOI/Al$ SGOI-MOS capacitor: (a) as-deposited and (b) annealed

shift (ΔV_{fb} = 0.36 V) is the result of a large number of interfacial trapped charges as the result of GeO_x formation in the IL according to the $Ge2p_{3/2}$ XPS results (not shown here). On the other hand, a well-behaved *C-V* curve is obtained in the annealed sample, as shown in Fig. 9 (b). The trapping and detrapping electrons almost disappear, and no obvious hysteresis exists between the positive and negative scans indicating that little interface trapped charges are located in the gate dielectric or at the interface between the gate dielectric and the top SiGe of FD SGOI. We believe that this difference between the as-deposited and annealed samples mainly results from the chemical state of the interfacial layer because of GeO_x incorporation into the IL of the as-grown film, while that of the annealed sample comprises a silicate layer. On the other hand, the annealing process is advantageous to the neutralization of the charges.

6. Conclusion

The recent progress made in our laboratory on our recent high-*k* materials research results is reviewed. The interfacial properties of high-*k* materials such as Ta_2O_5, ZrO_2, and HfO_2 deposited on Si were investigated and their dielectric properties were also discussed. The characteristics of Al_2O_3 gate dielectrics on fully-depleted SiGe-on-insulator (SGOI) were also described. The interfacial properties of these high-*k* films are obviously improved and it will promote the compatibility with ultra shallow junction techniques and accelerate the application of alternative high-*k* thin films in advanced gate dielectric fields.

Acknowledgments

The author thanks the members of the Plasma Laboratory as well as collaborators for their contributions. The work was supported by City University of Hong Kong Strategic Research Grant # 7001820.

References

[1]. M. Houssa: High-k Gate Dielectrics (IOP Publishing Ltd, 2004). chap. 1 p. 5.
[2]. *International Technology Roadmap for Semiconductors: 2005* (Semiconductor Industry Association, San Jose, CA, 2005).
[3]. A. P. Huang, and Paul K. Chu, *J. Appl. Phys.*, 97 (2005) 114106.
[4]. H. Ono, and K. I. Koyanagi, *Appl. Phys. Lett.*, 77 (2000) 1431.
[5]. A. P. Huang, S. L. Xu, M. K. Zhu,, G. H. Li, T. Liu, B. Wang, and H. Yan, *J. Cryst. Growth*, 255 (2003) 145.
[6]. A. Pignolet, G. M. Rao and S. B. Kurpanidhi, *Thin Solid Films*, 258 (1995) 230.
[7]. A. P. Huang, R. K. Y. Fu, and Paul K. Chu, *J. Cryst Growth.*, 277 (2005) 422.
[8]. L. Wang, K. Xue, J. B. Xu, A. P. Huang, and Paul. K. Chu, *Appl. Phys. Lett.*, 88 (2006) 072903.
[9]. Z. F. Di, M. Zhang, W. L. Liu, Q. W. Shen, S. H. Luo, Z. T. Song, C. L. Lin, A. P. Huang, and P. K. Chu, *Appl. Phys. Lett.*, 86 (2005) 262102-1.