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Electrical and interfacial characteristics of nanolaminate ($Al_2O_3/ZrO_2/Al_2O_3$) gate stack on fully depleted SiGe-on-insulator

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Abstract

The structural and electrical characteristics of a novel nanolaminate $Al_2O_3/ZrO_2/Al_2O_3$ high-*k* gate stack together with the interfacial layer (IL) formed on SiGe-on-insulator (SGOI) substrate have been investigated. A clear layered Al_2O_3 (2.5 nm)/ZrO_2 (4.5 nm)/Al_2O_3 (2.5 nm) structure and an IL (2.5 nm) are observed by high-resolution transmission electron microscopy. X-ray photoelectron spectroscopy measurements indicate that the IL contains Al-silicate without Ge atom incorporation. A well-behaved *C–V* behavior with no hysteresis shows the absence of Ge pileup or Ge segregation at the gate stack/SiGe interface.

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1. Introduction

It is well known that electron and hole mobilities are enhanced in strained Si and strained SiGe. In modulation-doped field effect transistors (MODFETs), electron and hole mobilities in Si under tensile strain and SiGe under compressive strain are 2200–2800 and 800–1050 $cm^2/V\,s$, respectively, exceeding the corresponding values in conventional Si by 3–5 times [1,2]. In particular, the hole mobility enhancement is more effective than that of electron, since conventional Si-CMOS performance is mainly limited by the lower current drivability of pMOSFETs. From this viewpoint, strained SiGe is a promising candidate for pMOSFETs in CMOS applications due to its high hole mobility [3]. At the same time, SOI has been incorporated into CMOS to achieve high-end performance because the use of a buried oxide (BOX) underneath bulk Si CMOS devices produces a number of benefits such

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as reduction of junction capacitances, increased circuit density due to tighter isolation, and reduced latch-up. Therefore, incorporation of strained SiGe channels into SiGe-on-insulator (SGOI) is one of the most promising p-channel device designs in high-performance CMOS applications [4].

The use of SiGe in strained SiGe-pMOSFETs has been plagued by problems such as poor gate oxide quality due to Ge segregation and serious degradation of the oxide properties during conventional thermal oxidation of the strained SiGe layers [5]. On the other hand, aggressive MOSFET device scaling in Si has led to an interest in the deposition of high dielectric constant (high-k) gate materials having low leakage current, good thermal stability, and interfacial characteristics comparable to those of a SiO_2/Si interface. Replacing the thermally grown SiO_2 with a deposited high-k dielectric also provides a viable solution for fabrication of SiGe-pMOSFETs because of absence of the high-temperature SiGe oxidation process. Recently, a novel nanolaminate $Al_2O_3/ZrO_2/Al_2O_3$ high-k gate stack has been proposed for Si-based CMOS due to its excellent thermal stability and electrical performance [6–8]. However, such a gate stack has hitherto not been extended to SiGe-based high-performance CMOS technology. Here, we report the structural and electrical properties of $Al_2O_3/ZrO_2/Al_2O_3$ gate dielectrics deposited on fully depleted SGOI substrate and the resulting interfacial layer (IL) is investigated in details to determine its potential in SiGe-pMOSFETs device applications.

2. Experimental procedures

The fully depleted strained SGOI substrate was fabricated by using the Ge condensation by oxidation technique [4]. This method was originally developed to form relaxed SGOI substrate for strained Si channel MOSFETs. However, T Tezuka [9] has found that relaxation can be suppressed if the initial SiGe thickness T_i is less than a critical value. During the oxidation and condensation procedures, the SiGe lattice constant parallel to the surface should be kept to this initial value in order to produce compressive strain in the SGOI layer. In this way, a strained SiGe layer can be successfully fabricated directly on the BOX layer. In this work, the thickness of the top SiGe and BOX layers were 25 and 380 nm, respectively. The $Al_2O_3/ZrO_2/Al_2O_3$ gate stack was deposited in an electron-beam evaporation system. High-purity sintered ZrO_2 and Al_2O_3 were evaporated by two electron guns and deposited on the SGOI substrate at room temperature (about 25 °C) and pressure of 10^{-6}–10^{-7} Pa. The $Al_2O_3/ZrO_2/Al_2O_3$ structure was deposited at rates of 0.3–0.5, 0.5–0.8, 0.3–0.5 Å/s, respectively. The relatively thick gate stack (~10 nm) prepared in this work is more suitable for the study of the IL composition by X-ray photoelectron spectroscopy (XPS). The samples were subsequently furnace annealed in N_2 at 450 °C for 30 min to neutralize the charge at the interfaces.

3. Results and discussion

High-resolution transmission electron microscopy (HR-TEM) was conducted using a CM200FEG at an operating voltage of 200 kV and resolution of 0.24 nm to probe the thickness and interfacial structure of the deposited gate dielectrics. Figs. 1(a) and 1(b) depict the cross-sectional TEM image of the high-k gate stack on SGOI structure. In Fig. 1(a), the $Al_2O_3/ZrO_2/Al_2O_3$ gate stack and an IL on the SGOI substrate is clearly shown and all four interfaces are very sharp. Fig. 1(b) shows that all the three high-k layers and the IL are amorphous. The thickness of the gate stack Al_2O_3 (2.5 nm)/ZrO_2 (4.5 nm)/Al_2O_3 (2.5 nm) is much larger than that of the IL (2.5 nm). The clear lattice image indicates the high quality of the SGOI substrate fabricated by the Ge condensation by oxidation technique. It is well known that an IL between Al_2O_3 and Si substrate is unavoidable [10], but such a study on SiGe or SGOI substrate has not been reported. Here, we show the structural and electrical properties of the IL between Al_2O_3 and SGOI substrate.

X-ray photoelectron spectroscopy was conducted on the Physical Electronics PHI 5802, which used a monochromatic aluminum X-ray source. Fig. 2 shows the measured Al 2p, Si 2p, Ge 2p3/2, and O 1 s peaks (sputtering rate is about 0.25 nm/cycle) in the annealed $Al_2O_3/ZrO_2/Al_2O_3$/IL/SGOI structure. Figs. 2(a) and 2(d) show strong signature of typical Al_2O_3 bonding, namely the shifted Al 2p peak at 74.2 eV and shifted O 1s peak at 531.0 eV. At the 35th sputtering cycle, an obvious shift to a high binding energy can be observed in both the Al2p and O1s peaks, suggesting the formation of an IL composed of different materials than Al_2O_3. As shown in Fig. 2(c), almost no Ge–O bond can be

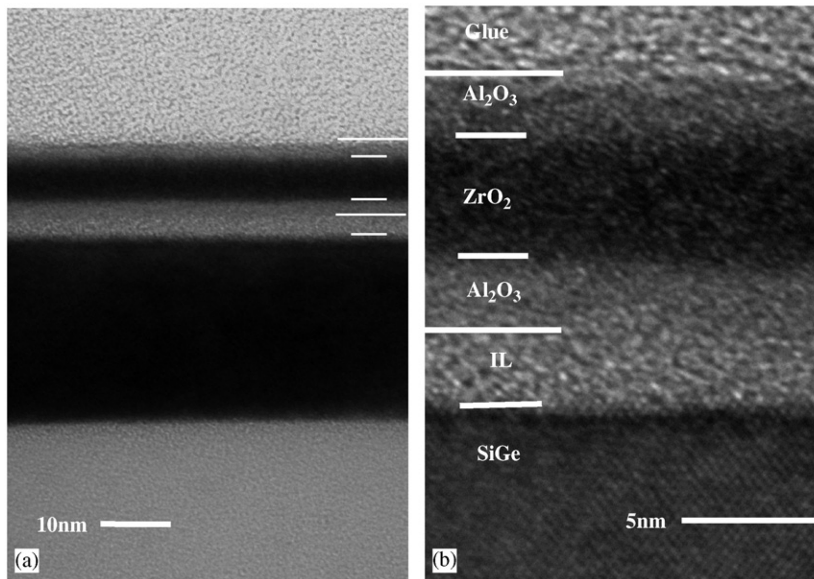

Fig. 1. TEM micrograph of $Al_2O_3/ZrO_2/Al_2O_3$ high-*k* gate stack fabricated on SGOI substrate showing the formation of an interfacial layer: (a) cross-section and (b) high-resolution cross-section.

detected at the interface. From the intensities of the XPS peaks of the Ge–Ge bonds near the interface, it can be concluded that there is no Ge pileup or Ge segregation [16] at the gate stack/SGOI interface. In Fig. 2(b), the shifted Si2p peak is at ~102.4 eV corresponding to a shift of about 3.1 eV from pure Si. It is known that the binding energy difference between SiO_2 and Si is about 4.4 eV [11]. A lower binding energy with respect to SiO_2 indicates that the IL composition is silicate-like thereby signifying the formation an Al-silicate IL. This composition is also consistent with the peak shifts at the 35th sputtering cycle in the Al 2p and O 1s signals at the interface shown in Figs. 2(a) and 2(d) similar to Al_2SiO_5 [12].

To explain the formation of the Al-silicate IL without Ge atom incorporation, inference may be made from the oxidation phenomenon of the SiGe alloys similar to that in the SGOI substrate fabrication process. Preferential oxidation of Si relative to Ge occurs because of the more negative Gibbs free energy to form SiO_2 than GeO_2 [13]. The standard Gibbs free energies of formation ($\Delta_f G^0$) at 298.15 K for Al_2O_3, SiO_2, and GeO_2 are −1582.3, −856.3, and −521.4 kJ mol^{-1}, respectively [14]. Neglecting the small temperature influence on the Gibbs free energy change (ΔG), the reaction GeO_2(cr) + Si(cr) → SiO_2(cr) + Ge(cr) should result in a large negative Gibbs free energy in the temperature range used in this work. From the perspective of thermodynamics, Si is more reactive than Ge. Therefore, only Si is oxidized and Ge atoms are rejected from the IL subsequently diffusing into the SiGe layer of SGOI substrate during annealing. The diffusion coefficient of Ge in SiGe is very large and the amount of the rejected Ge atoms is quite small thereby not affecting the quality of the SiGe layer.

The electrical properties of the gate dielectric stack are studied using an Al electrode on the $Al_2O_3/ZrO_2/Al_2O_3$/IL/SGOI structure (SGOI-MOS capacitor). Fig. 3 shows the typical high-frequency (1 MHz) capacitance–voltage (*C–V*) characteristics of the as-deposited and annealed (450 °C, 30 min) gate dielectric stacks with a physical thickness ~12.0 nm. In Fig. 3(a), the hysteresis loop in the counterclockwise direction exhibits a relatively large flat band voltage shift ($\Delta V_{fb} = 1.58$ V) indicating a large number of interfacial trapped charges. On the other hand, the trapping and detrapping phenomena cannot be observed in the annealed sample as shown in Fig. 3(b). A well-behaved *C–V* behavior is obtained with a relatively low flat band voltage shift ($\Delta V_{fb} = 0.15$ V) between the positive and negative scans. Almost no hysteresis exists in the entire scan, showing that little interface trapped charges are located in the gate stack or at the interface between the gate stack and

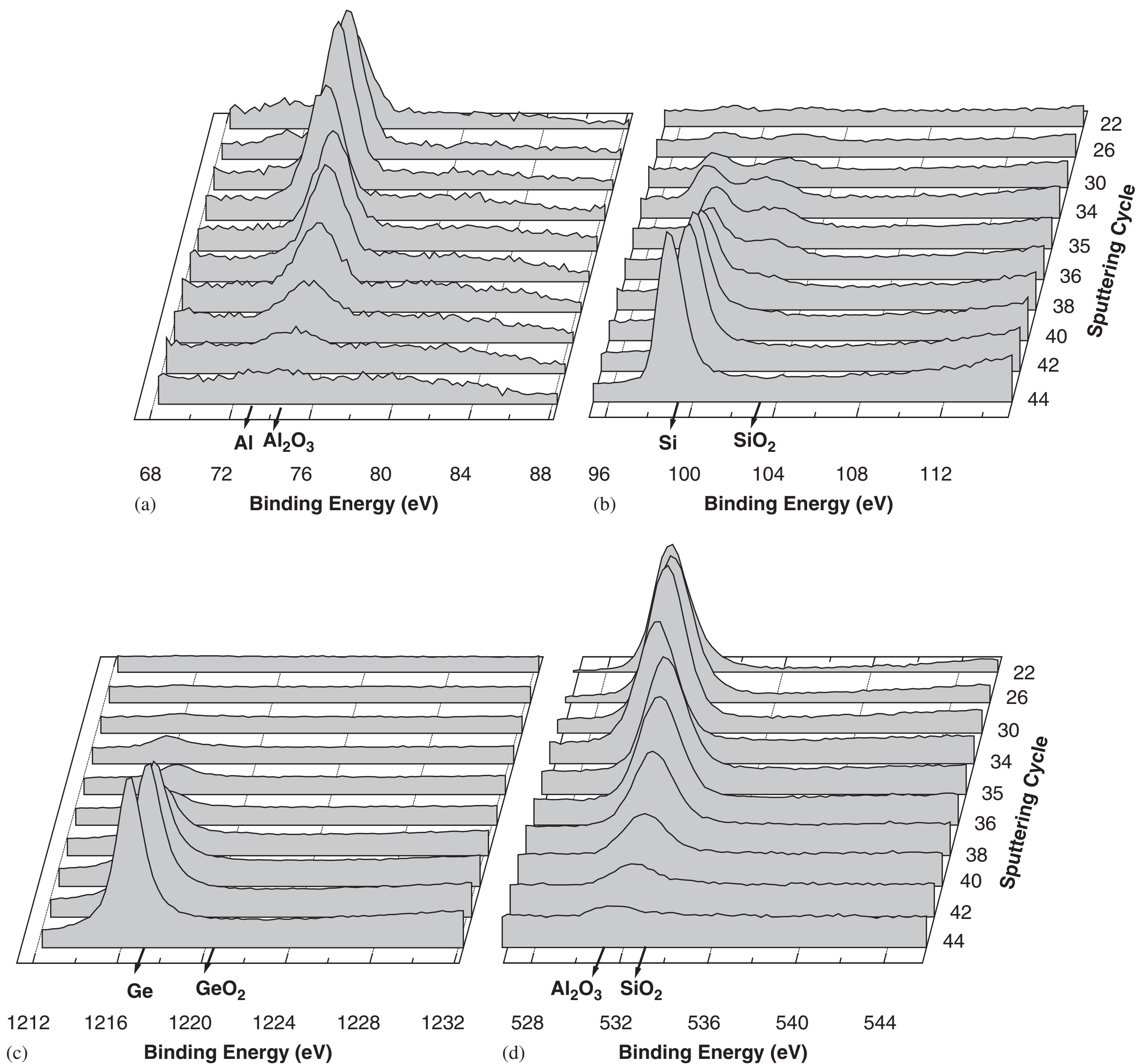

Fig. 2. High-resolution XPS spectra acquired from the $Al_2O_3/ZrO_2/Al_2O_3$/IL/SGOI structure: (a) Al 2p, (b) Si 2p, (c) Ge 2p3/2, and (d) O 1s.

the top SiGe layer of SGOI. The flat band voltage shift can be estimated by the relationship $\Delta V_{fb} = (d/\varepsilon_s)Q_t$ [15], where d is the distance between the interfacial trapped charge and the gate electrode, Q_t is the interfacial trapped charge density, and ε_s is the dielectric constant of the gate stack. Therefore, 90% of the interfacial trapped charges have been neutralized during the annealing process, and Ge pileup or Ge segregation [16] at the gate stack/SGOI interface is eliminated due to Ge diffusion.

4. Conclusion

We report the physical and electrical properties of a novel nanolaminate $Al_2O_3/ZrO_2/Al_2O_3$ high-k gate stack together with the resulting interfacial layer formed on the SGOI substrate. The physical thickness and structure of the gate stack (9.5 nm) and Al-silicate IL (2.5 nm) are studied by HRTEM. The composition and the formation of Al-silicate IL without Ge atom incorporation are investigated by XPS. A well-behaved C–V behavior with no

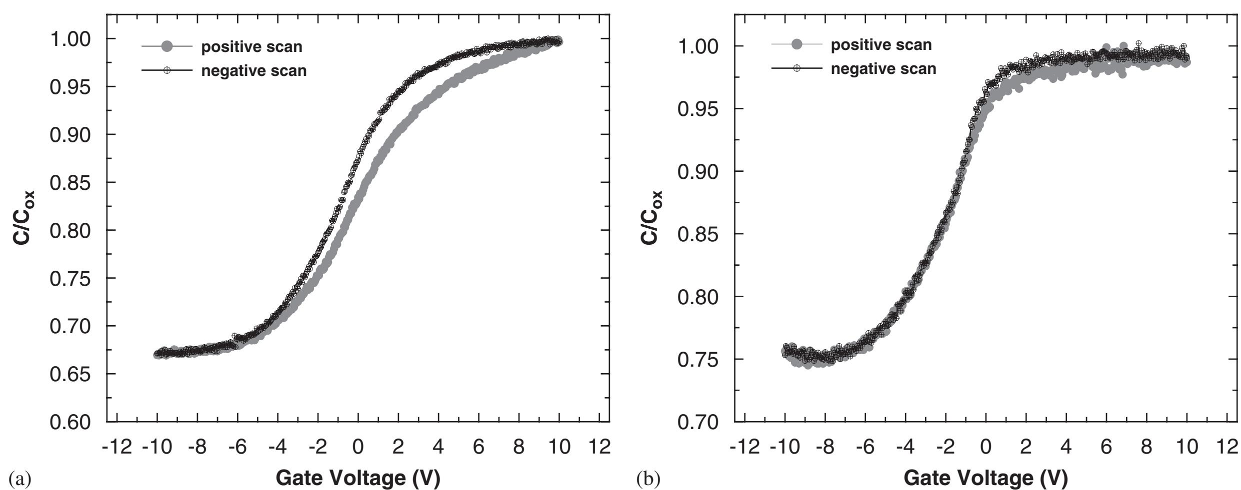

Fig. 3. High-frequency (1 MHz) *C–V* characteristics of the Al/Al_2O_3/ZrO_2/Al_2O_3/IL/SGOI MOS capacitors: (a) as-deposited and (b) 450 °C annealed.

hysteresis indicates the absence of Ge pileup or Ge segregation at the gate stack/SiGe interface. The Al_2O_3/ZrO_2/Al_2O_3 high-*k* gate stack is thus a promising gate dielectrics in future SiGe-based devices.

Acknowledgments

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