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Fabrication of silicon-on-SiO_2/diamondlike-carbon dual insulator using ion cutting and mitigation of self-heating effects

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A diamondlike-carbon (DLC) layer was used to substitute for the buried SiO_2 layer in silicon on insulator (SOI) to mitigate the self-heating effects in our previous study. However, we discovered drawbacks associated with the inferior Si/DLC interface, inadequate thermal stability as well as carbon-silicon interdiffusion at the Si/DLC interface that could hamper future application of this silicon-on-diamond structure to microelectronic devices. In this work, we introduced a silicon dioxide barrier layer between the Si film and DLC buried layer to form a silicon-on-SiO_2/DLC dual-insulator structure to tackle these problems. Cross-sectional high-resolution transmission electron microscopy reveals that the Si/insulator interface is atomically flat and the top Si layer has nearly perfect crystalline quality. The SiO_2/DLC dual-insulator layer retains excellent insulating properties at typical complementary metal oxide silicon processing temperatures. Numerical simulation reveals that the negative differential resistance and channel temperature are significantly reduced compared with those of the same metal oxide semiconductor field effect transistors fabricated in conventional SiO_2-based SOI, suggesting that the silicon-on-dual-insulator structure can alleviate the self-heating penalty effectively.
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Current integrated circuit (IC) designs are quickly approaching their physical limits[1] and the silicon-on-insulator (SOI) technology can provide some of the solutions in the sub-100-nm technology node.[2,3] However, a wider application of SOI in high-power ICs is hampered by the self-heating effect caused by the poor thermal conductivity of the SiO_2 buried layer.[4] Thus, exploration of alternative buried insulators with better thermal conductivity to more effectively remove the heat during device operation is needed.[5]

Diamond is a potential replacement for SiO_2 in SOI because of its inherent insulating properties (above $10^{13}\ \Omega\,\mathrm{cm}$) coupled with the best thermal conductivity ($\sim 20\ \mathrm{W\,cm^{-1}\,K^{-1}}$) found in nature.[6] The ion-cutting technique that involves hydrogen-induced layer cleavage and wafer bonding has become one of the popular SOI fabrication techniques and can be applied to the synthesis of silicon on diamond (SOD). However, prior studies[7,8] have revealed that the large surface roughness of the polycrystalline diamond film prohibits direct bonding to silicon wafers without extensive polishing and surface treatment. Diamondlike carbon (DLC) having an amorphous structure has been proposed to be a low-cost substitute for diamond. In our previous study,[9] we replaced the buried silicon dioxide layer with DLC to produce the SOD structure. However, despite the fabrication success, we noticed several intrinsic problems. First of all, the quality of the Si-DLC interface is worse than that of the Si$-$$SiO_2$ interface, though the surface of the DLC film synthesized by plasma immersion ion implantation and deposition (PIII&D) is very smooth and uniform, enabling successful wafer bonding. This may affect device performance as it is well known that the silicon-insulator interface impacts the surface channel mobility due to Coulomb scattering as well as interface roughness scattering.[10] Secondly, the thermal stability of the SOD structure needs to be further improved. Thirdly, the diffusion coefficient of C in Si is large,[11,12] and so it is difficult to suppress carbon-silicon interdiffusion at the Si/DLC interface, particularly at the high temperatures

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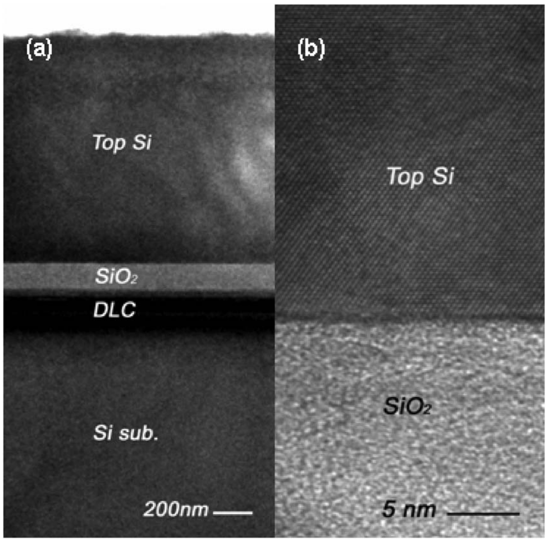

FIG. 1. (a) TEM micrograph of the SiO_2/DLC SODI structure. (b) High-resolution TEM micrograph of the interfacial region between the top Si layer and buried insulator structure showing a sharp Si/SiO_2 interface and defect-free crystalline Si layer.

used in conventional complementary metal oxide semiconductor (CMOS) processes. Here, we propose a solution by insertion of a silicon dioxide barrier layer between the top Si film and DLC buried layer to form a silicon-on-dual-insulator (SODI) structure to smooth the interface, enhance the thermal stability, and mitigate C diffusion while retaining the advantages offered by DLC with respect to the self-heating effect.

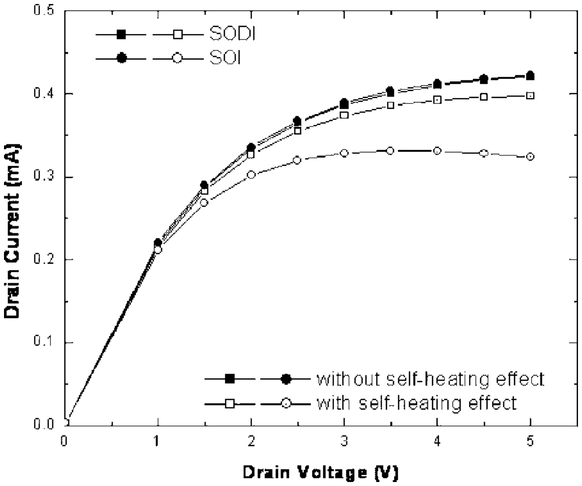

FIG. 3. Simulated output characteristics of conventional SiO_2-based SOI and SODI devices.

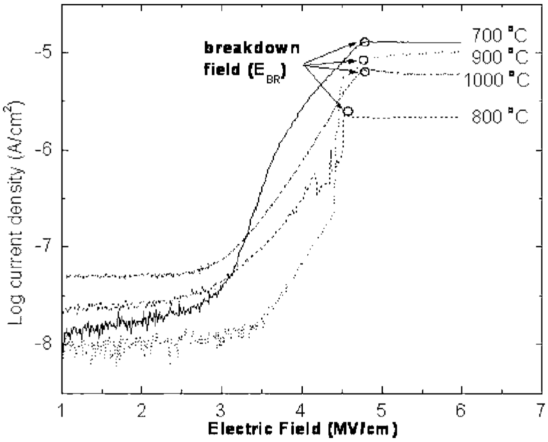

FIG. 2. Influence of the annealing temperature on the breakdown electric fields of the SODI structure.

A 200 nm thick amorphous DLC film was deposited on a 100 mm *p*-type Si (100) wafer using PIII&D.[13–15] An acetylene (20 SCCM)—argon (5 SCCM) mixture was introduced into the vacuum chamber of a multipurpose PIII instrument (SCCM denotes cubic centimeter per minute at STP).[16] Addition of argon enhanced the plasma discharge. Film deposition was carried out at a working pressure of 8×10^{-4} Torr using 13.56 MHz, 500 W radio frequency (rf). The applied voltage, repetition rate, and pulse width were −20 kV, 40 Hz, and 400 μs, respectively. The deposition time was 180 min. This DLC-coated wafer became the acceptor wafer in the subsequent bonding experiment. A Si donor wafer with a 160 nm thick thermal oxide was implanted with 6×10^{16} cm^{-2} hydrogen ions at 140 keV with a 7° tilt at room temperature. Afterwards, both the acceptor and donor wafers were cleaned with $H_2SO_4:H_2O_2$ (10:1) at 120 °C for 10 min, followed by rinsing in de-ionized (DI) water and spin drying. The surfaces were then activated in 400 W oxygen plasma (oxygen pressure of 1.3 Torr) at 100 °C for 60 s. After dipping in a modified RCA-1 solution ($NH_4OH:H_2O_2:H_2O=1:6:30$) at 70–75 °C for 60 s followed by DI water rinsing and spin drying, the DLC-coated acceptor wafer was bonded to the hydrogen-implanted SiO_2-coated donor wafer at room temperature. The bonded pair was heated to 120 °C for 2 h in air and then to 200 °C for 10 h to strengthen the bonding. Afterwards, the bonded pair was annealed at 300 °C for 2 h under nitrogen and finally heated to 450 °C for 10–15 min. During this final stage, H-induced microcracks were formed in the H-implanted SiO_2-coated donor wafer, eventually leading to layer cleavage and transfer of the SiO_2/Si layer onto the DLC-coated acceptor wafer, thereby producing a SODI structure.

Cross-sectional transmission electron microscopy (TEM) was performed and Fig. 1(a) shows direct evidence of the successful fabrication of the SODI structure. The thickness of the top Si layer is about 1070 nm, and the buried insulator includes 160 nm of SiO_2 and 200 nm of DLC, giving a total thickness which is quite common for commercial SOI wafers. In the high-resolution image of the Si/insulator interface depicted in Fig. 1(b), the Si layer retains high crystalline quality and no discernable defects can be observed.

It is well known that a high annealing temperature accelerates graphitization of DLC, increasing its electrical conductivity, although our previous work shows that buried DLC exhibits better thermal stability than exposed DLC.[17] A resistive buried layer is imperative to the optimal operation of SOI devices and so we measured the breakdown electric fields of our SODI sample at various temperatures to determine the thermal stability. As shown in Fig. 2, even at an annealing temperature as high as 1000 °C, the breakdown field of 4.6±0.1 MV/cm remains more or less unchanged. This is a substantial improvement over our previous SOD structure which shows significant degradation at 1000 °C.[9] The enhanced property is believed to be due to two reasons. First of all, the SiO_2 layer has high thermal stability. Secondly, the SiO_2 layer impedes hydrogen outdiffusion from the underlying DLC layer. Hydrogen outdiffusion was observed in our previous experiments[17] to be the primary reason for early graphitization. It is also noted that the insulating property of this SiO_2/DLC dual layer is better than that of a typical buried oxide produced by separation by implantation of oxygen (SIMOX).[18]

In order to investigate the benefits offered by the DLC layer with regard to the mitigation of the self-heating effects, we performed numerical simulation to compare the electrical characteristics and temperature distribution between metal oxide semiconductor field effect transistors (MOSFETs) fabricated in conventional SOI and SODI. The analysis was carried out using a two-dimensional device simulator MEDICI.[19,20] The substrate has a p-type doping concentration of $10^{18}\ \mathrm{cm}^{-3}$ and n-type source and drain doping of $10^{20}\ \mathrm{cm}^{-3}$. The channel length is 0.2 μm, and the thicknesses of the gate oxide, top silicon, and buried SiO_2/DLC are 5, 1070, and 160/200 nm, respectively. The thermal conductivities of Si, DLC, and SiO_2 used in our simulation are 145, 2000, and 1.4 W/m K, respectively.[9] All the geometrical parameters of the MOS device in conventional SiO_2-based SOI are identical with the exception of the buried insulator which consists of 360 nm thick pure SiO_2. The output characteristics derived from the devices (SOI and SODI MOSFETs) with and without the self-heating effect are compared in Fig. 3. The output characteristics of the MOSFET show the drain current I_D versus the drain-source voltage V_{DS}, with the gate-source voltage V_{GS} as the parameter. The gate bias is held at 5 V, which is a common value used in high-power MOS devices in SOI. The drain bias is ramped up from 0 to 5 V. This operating region tests the high-current operation and whether the self-heating effect occurs in regular usage. In the SOI device, neglecting the effect of self-heating overestimates the current by about 31% at V_{GS}=5 V and V_{DS}=5 V. However, this value is reduced to 6.3% in the SODI device, indicating that the SOI device shows strong negative differential resistance (NDR) compared with the SODI device when the self-heating effect is considered. It is well known that NDR stems from mobility reduction caused by the elevated lattice temperature.[21] By examination of the self-heating effect (based on NDR shown in the I_{DS}-V_{DS} curves), it can be concluded that the relatively low thermal conductivity of the buried SiO_2 layer in the conventional SOI device leads to insufficient heat dissipation resulting in mobility degradation and obvious NDR. On the other hand, the thinner SiO_2 layer (160 nm) together with the underlying DLC layer in the SODI mitigates this effect. Consequently, only a slight self-heating effect is found in the SODI device under the same operating conditions. Figure 4 shows the three-dimensional (3D) temperature distributions of the two devices under the same operating conditions, and the results are consistent with the output characteristics. The x and y axes represent the horizontal and vertical dimensions of the device, respectively. In the SOI device, even though the substrate temperature remains at 300 K (room temperature), the channel temperature rises to 510 K during operation due to the self-heating effect. In contrast, the channel temperature in the SODI device only rises to 360 K which is only slightly higher than the substrate temperature. Our results thus show that SODI which encompasses the advantages of both SiO_2 (bonding ease, interface abruptness, and so on) and DLC (high heat conductance) is a possible replacement for conventional SiO_2-based SOI.

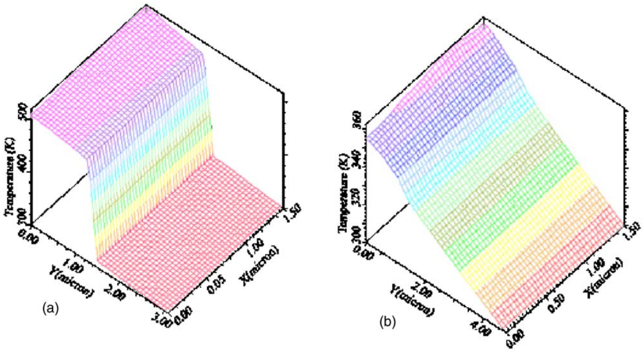

FIG. 4. (Color online) Simulated 3D temperature distributions of devices in (a) SiO_2-based SOI and (b) SODI.

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