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Recent Developments and Applications of Plasma Immersion Ion Implantation (PIII)

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ABSTRACT
Plasma immersion ion implantation (PIII) is an established technique in some niche microelectronics applications such as synthesis of silicon-on-insulator. In other applications such as shallow junction formation by plasma doping, trench doping, and others, PIII possesses unique advantages over conventional techniques. There have been significant developments in these areas and recent developments in plasma doping, direct-current plasma immersion ion implantation (DC-PIII) that excels in planar sample processing, as well as PIII of insulating materials are presented.

INTRODUCTION
Plasma immersion ion implantation (PIII) was first introduced in the 1980s to circumvent the line-of-sight restriction of conventional beam-line ion implantation (1,2). PIII also offers advantages such as high efficiency, large area and batch processing, as well as small instrument footprint. Fig. 1 illustrates some of the processes occurring in the PIII chamber demonstrating the versatility and potential problems of the technique. In addition to metallurgical engineering, PIII excels in semiconductor and microelectronics processing as well as biomedical engineering (3,4). The most widely studied semiconductor applications of PIII are shallow junction formation by plasma doping (5-11), production of silicon-on-insulator (SOI) substrates by either PIII / ion-cut or separation by plasma implantation of oxygen (SPIMOX) (12-19), conformal trench doping (20), hydrogenation of polysilicon thin films used in flat-panel displays (21), as well as fabrication of thin oxide on SiGe, low dielectric constant (low-k), and III-nitride materials (22-24).

In this paper, recent developments and applications of PIII are described.

PLASMA DOPING
PIII is a competing doping technique in ULSI (ultra-large-scale integration). Modern silicon microelectronic devices require ultra-shallow source / drain (S/D) extensions to reduce short-channel effects and enhance the performance. Shallow junctions can be accomplished using low energy conventional beam-line ion implantation and rapid thermal annealing. In spite of recent progress on hardware improvement (25), conventional beam-line ion implantation still suffers from small throughput and poor beam performance as a low-energy tool (26,27). Hence, PIII, also called plasma doping (PD), has attracted much attention. As an ultra-shallow junction fabrication technique, PIII (PD) has been demonstrated for both n-type and p-type ultra-shallow junctions. In order to improve the process, much work is being conducted on related issues such as high activation efficiency, reduction of damage, improvement of dopant profile steepness, and enhancement of transistor performances. However, PD is still not a mature technique from the commercial perspective and a few practical issues such as dosimetry accuracy, tilt requirements, and precision must still be solved (28).
Fig. 1: Processes occurring in a PIII chamber.

Fig. 2 shows some other typical PIII applications in ULSI silicon processing. Examples shown here include trench sidewall doping of deep trench-based and stack capacitor-based dynamic random access memory (DRAM), gate oxide processing, as well as polysilicon gate doping. A deep trench capacitor used as charge storage elements in DRAM consists of a thin insulating node fin and capacitor electrodes, and the n-type region in the p-type Si substrate surrounding the trenches constitutes the buried-plate electrode. In spite of miniaturization, the charge storage capacity of the DRAM capacitors should be maintained. In addition, as the node dielectric thickness diminishes, the n-type dopant
concentration on the electrodes must be increased to mitigate the depletion capacitance. PIII as a conformal trench sidewall doping technique is thus very attractive and the process has been demonstrated in a deep trench with an aspect ratio of 35:1. Fig. 3 shows a secondary electron micrograph of an array in a DRAM cell comprising 6 μm deep and 0.175 μm wide trenches. The PIII process is conducted using AsH₃ plasma with a plasma density of 10¹⁷ cm⁻³. The DRAM cells are biased at 1 or 7 kV and the implant doses range from 1x10¹⁵ to 6x10¹⁷ atoms-cm⁻².

Fig. 2: Application examples of PIII to ULSI silicon processing (27).

Fig. 3: SEM micrograph of deep trench array in a DRAM cell (27).
Hydrogen ion implantation is at present used commercially to produce silicon-on-insulator (SOI) (29,30) and has been extended to perform layer transfer in other materials (31,32). As shown in Fig. 4, the ion-cut process requires high dose hydrogen ion implantation to create micro-cavities along the projected range of the implant. Upon annealing, the stress imposed by the expansion and coalescence of these micro-cavities causes delamination of the wafer along the projected range of the implanted ions. In the silicon ion-cut process illustrated here, the implanted or donor wafer is bonded to another silicon or acceptor wafer before annealing and the cleaved silicon film is transferred to the acceptor film. If the acceptor film has a surface oxide layer, the resulting structure becomes a silicon-on-insulator. As the required hydrogen dose for the layer transfer process is quite high, typically in the mid $10^{17}$ atoms/cm$^2$, PIII is more economical than conventional beam-line ion implantation. In addition to innovations in hardware, the success of PIII stems from intensive research and subsequent improvement on the uniformity of ion dose and implant energy as well as processing issues such as contamination (33-35).

I. Hydrogen-PIII

![Diagram of Hydrogen Plasma and Implant Layer]

II. Wafer Bonding

![Diagram of Donor and Receptor Wafers with Hydrogen Implant Layer]

III. Ion-cut

![Diagram of Transferred Layer and SOI Structure]

Fig. 4: Schematic of Hydrogen PIII ion-cut process.
In the ion-cut process, the important parameter is the depth of the hydrogen implant provided that a critical dose has been implanted. Hydrogen PIII is typically performed in mTorr or sub-mTorr pressure to ensure non-collisional conditions in which the ion mean free path is much larger than the ion-matrix sheath thickness. However, low energy ions implanted during the rise and fall times of the voltage pulses can introduce defects affecting the yield of the ion-cut process (36-38). During the short but finite rise and fall times of each voltage pulse, the ion acceleration energy is reduced, resulting in a low energy component in the impant distribution. In addition, when a negative high voltage pulse is imposed, the vacuum chamber, sheath, and circuit inherently induce an equivalent capacitive load on the power modulator and give rise to a displacement current (39). This displacement current generates extra heating to the wafer and sample stage, and metal impurities can diffuse from the contact interface and sample stage into the wafer, and are subsequently driven into the wafer at higher temperature. Therefore, cooling is sometimes required in the implantation process. These effects are deleterious in the PIII - ion cut and PIII - SIMOX techniques (40). Hence, in order to reduce the effects of the voltage pulse rise and fall times, direct-current PIII has been proposed (41-44).

Fig. 5 displays a DC-PIII apparatus consisting of a radio frequency (RF) plasma source. A conducting grid, made of a compatible material to avoid contamination (e.g. a silicon coated mesh for implanting silicon wafers), divides the chamber into two halves. In the lower part, a strong electric field is formed between the negatively biased wafer stage and the boundaries created by the grid in the lower part of the chamber walls. The upper part confines the plasma since the grounded grid atos the expansion of the ion sheath. In this way, a continuous low-pressure discharge can be maintained in the volume above the grid without plasma extinction even at high sample voltage. Without the grid, the plasma sheath may prograde all the way to the top of the PIII chamber thereby extinguishing the plasma. Positive ions diffuse into the lower part through the grid and are implanted into the top of the wafer.

Particle-in-cell (PIC) simulation shows that the ion paths will not change with the negative voltage applied to the wafer stage, mass, and charge states of the ions, provided that their initial velocity is small compared to the electric field (45). The ion trajectory is determined by the velocity vector that in turn changes with the acceleration vector created by the force field in space. The direction of the ion does not depend on the charge state and mass of the ions. Hence, by varying the change state of the ion and applied voltage, the impact energy can be altered, and by varying the ion mass, the final velocity of the ion can be changed. However, if the ions have a large initial drift velocity compared to the maximum velocity created by the applied voltage, they will pass through a different local field structure.

The dose and energy uniformity along the implanted wafer are important issues for PIII, and as aforementioned, there are many low energy ions introduced into the wafer during the rise and fall times of each negative voltage pulses. In the DC-PIII mode, the ion impact energy is constant since the ions are accelerated directly from the grid to the wafer stage. The uniformity of the ion dose on the wafer depends on two factors: the uniformity of the incident ion current and impact angle. In the DC mode, the implantation area is totally determined by the ratio of the radius of wafer stage r, the radius of the vacuum chamber R, the distance between the wafer stage and grid H, and thickness of the wafer stage D. The projected area from the grid to the wafer stage determines the incident dose into the wafer. Actually, the smaller H is the closer is the ratio of the projected area to the implanted area to 1 and the better is the incident dose uniformity. However, the shorter the distance between the anode (grid) and cathode (wafer stage), the higher is the electric field which may lead to breakdown at high implantation voltage. The impact angle at the edge can be made normal by changing the dimension of the wafer stage. For instance, a thicker wafer stage can smooth out the electric field at the edge. In PIII, the ions are accelerated from the ion sheath and the impact angle is determined by the topography of the sheath. Hence, the retained dose and impact energy in the DC mode can be made more uniform by choosing the suitable internal dimensions of the lower part.
Pill experiments are usually conducted at very low gas pressure to achieve high impact energy, for example, lower than 0.1 mTorr. Hence, a high intensity plasma source such as an ECR (electron cyclotron resonance) plasma source is necessary for high ion dose DC-Pill. Such an apparatus is displayed in Fig. 6. To determine the ion energy distribution and dose uniformity in this setup, RBS (Rutherford backscattering Spectrometry) analysis was done on a silicon wafer implanted by argon DC-Pill at 30 kV. The argon depth profiles at the center and edge of the wafer are shown in Fig. 7. The data agree well with the simulation result of TRIM (46) (projected range is 36.6 nm and longitudinal straggling is 14.6 nm), thereby verifying that the ion impact energy agrees well with the DC voltage. The argon depth profile reveals that the ion energy is monoenergetic. The calculated doses at the center and side of the 75 mm wafer are 2.97×10^{16} cm^{-2} and 2.52×10^{15} cm^{-2}, respectively. The dose uniformity can be improved by using a more uniform plasma source and better chamber geometry. The results unequivocally illustrate that the dose rate and electrical power efficiency are improved by DC-Pill. For instance, the dose rate can be as high as 1×10^{13} cm^{-2} min^{-1} and the electrical power consumption can be reduced to about one quarter of that in pulsed PIII.
To enhance the efficacy of the DC-PIII process, the grid separating the vacuum chamber can be biased. The process changes the plasma density in the upper chamber and modifies the plasma topography along the grid surface. Our results show an enhanced extracted ion current density from the plasma and suggest specific optimal process windows (47). In a more recent study (48), the implanted area is shown to increase with the radius of the extraction hole and wafer stage, but decreases with a larger distance between the grid and sample. The effects of the extraction hole radius are the largest, followed by the placement of the sample to the conducting grid. The wafer stage poses the smallest influence but a proper wafer stage dimension improves the lateral implant dose and incident angle homogeneity. Simulation and experimental results suggest optimal ratios of these parameters for each wafer size.
Fig. 7: Argon depth profiles of the center and the edge of the 75 mm silicon wafer derived from RBS data acquired from the argon DC-PIII silicon wafer.

**PILL OF INSULATING MATERIALS**

Attempts to implant dielectric substrates using PIII have encountered intrinsic technical problems. The common PIII approach is to place the dielectric sample on a conductive substrate holder and apply high voltage pulses to the holder. However, the magnitude of the potential at the dielectric–plasma interface induced by applying a potential to the rear surface of the dielectric is reduced by a combination of capacitive voltage division and charge accumulation due to the introduction of positive ions and emission of secondary electrons (49). The insulating substrate that is positioned on the conducting target holder cannot rise to the full (negative) pulse bias potential and consequently, the energy of the incident ions is less than the full pulse voltage. As a result, the effective dielectric thickness of the substrate and applied pulse length and frequency that can be used in practice are limited. In severe cases involving large pieces of bulk insulators, the surface potential is significantly reduced and instrumental arcing may become too difficult to overcome. For thinner dielectric samples, surface charging broadens the energy distribution of incident ions in addition to the effects of the rise or fall times of the negative pulses (50).

Surface charging is also brought about by secondary electron emission. The discharge time scale of the charged insulator surface can be on the order of 20 μs and a combination of short pulse duration, high pulse frequency, and low plasma density can be beneficial from the viewpoint of increasing the ion implantation energy.

In cases where the insulating substrates are thick, alternative approaches must be adopted. The obvious one is the use of a sacrificial conductive surface layer (51). In this method, thin conducting films are
Plasma immersion ion implantation has found a number of exciting applications. Plasma doping is a potential alternative to conventional beam-line ion implantation in trench doping and shallow junction formation. Hydrogen PIII as practiced in the layer transfer technology has gained acceptance due to recent improvement in the ion dose and energy uniformity as well as contamination control. The advent of DC-PIII obviates the need of the complicated and expensive power modulator and significantly reduces the instrumentation cost and footprint. This novel technique may find its way into commercial SOI fabrication and other semiconductor processes. The use of mesh-assisted PIII greatly expands the applications to insulating materials.
Fig. 9: Nitrogen depth profiles acquired by SIMS from plasma implanted SiO$_2$ samples with and without the grid.

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