

Direct current plasma implantation using a grounded conducting grid

Dixon T. K. Kwok, Xuchu Zeng, Chung Chan,^{a)} and Paul K. Chu^{b)}

Department of Physics & Materials Science, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong

(Received 18 October 1999; accepted for publication 2 February 2000)

A novel plasma implantation technique performed in a low pressure steady state dc mode utilizing a grounded conducting grid on top of the wafer stage is presented. By numerically simulating the ion paths by the particle-in-cell method, it is observed that the ion paths are optimized for certain implant geometry. In the optimal configuration, the directional angle of the acceleration vector does not depend on the mass and charge state of the ions, and the ratio of the partial differential of the scalar potential ϕ along the radial and longitudinal directions remains constant for varying applied voltages. The retained dose and impact energy uniformity are totally determined by the ratio of the radius of the wafer stage r , radius of the vacuum chamber R , distance between the wafer stage and the grid H , and thickness of the wafer stage D . The optimal ratio is $r:R:H:D = 1:4:2.5:2$, that is, suggesting a disk shape vacuum chamber, which is quite different from that of a conventional plasma immersion ion implanter. In addition to retaining the large area and parallel processing advantages of plasma immersion ion implantation (PIII), the implantation energy can be extended far beyond the limit of PIII as the technique obviates the use of the power modulator, which not only limits the implantation energy but also is the most expensive and technologically complex hardware component in a PIII system. © 2000 American Institute of Physics. [S0021-8979(00)08109-3]

I. INTRODUCTION

Plasma immersion ion implantation (PIII) is a versatile materials fabrication and surface treatment technique.¹⁻⁴ Its nonline-of-sight advantage renders it an excellent technique to enhance the properties and performance of large and irregular-shaped industrial components.^{1,5-7} For example, it is being applied to synthesize silicon-on-insulator substrates for low-power, high-speed complementary metal-oxide-silicon microelectronics chips.^{1,8,9} In the ion cut process, PIII is an efficient and economical approach to implant a high dose of hydrogen into a silicon wafer, and as the implantation time is independent of the wafer diameter, it is more appealing for larger wafers.

PIII differs from conventional beam-line implantation in several aspects. In beam-line ion implantation, the ions are accelerated by the electric field and filtered according to their mass-to-charge ratios. On the other hand, in PIII, the target is immersed in the plasma and biased by a series of negative voltage pulses. When the target is negatively biased, electrons are repelled away leaving a sheath of heavy positive ions. An electric field builds up between the sheath boundary and target surface, and ions are accelerated toward the target. To maintain a continuous flow of ions, the ion sheath expands until the end of the negative pulse. At high implantation voltage, the plasma will be extinguished if the sheath touches the wall of the vacuum chamber. This happens when the vacuum chamber (distance between the target and plasma source) is too small, the plasma density is too low, or the

voltage pulse is too long. These constraints, together with the limitation of the power modulator, impose a practical maximum voltage in PIII experiments and render the technique inadequate for the fabrication of thick (separation by implantation of oxygen (SIMOX)) materials, for instance. It should also be noted that in PIII, the local impact angle of the ions depends on the shape of the target.

There are several considerations for using negative voltage pulses in semiconductor PIII applications. When a negative high voltage pulse is imposed, the vacuum chamber, sheath, and electrical circuit inherently induce an equivalent capacitive load on the modulator inevitably giving rise to a displacement current.¹⁰ That is, a displacement current occurs due to the changing voltage, sheath capacitance, and circuit loads. The additional displacement currents generate extra heating to the wafer and sample stage. Deleterious metal impurities can diffuse from the contact interface and sample stage into the wafer, and are subsequently driven into the wafer at higher temperature. Therefore, cooling is sometimes required during the implantation process. During the short but finite rise and fall times of each voltage pulse, the ion acceleration energy is reduced, resulting in a low energy component in the implant distribution. Both of these effects are disadvantages in the ion cut and PIII-SIMOX techniques.¹¹

To mitigate these effects, we can elongate the pulse width to 100 μs or longer¹¹ or more ideally operate in the direct current (dc) mode, i.e., implanting the wafer at a steady-state Child-Langmuir law sheath. However, dc operation at high voltage requires a large vacuum chamber as the ion sheath can expand to the top of the discharge system causing plasma extinction. Since the chamber size is usually limited, in order to maintain a long pulse duration of pulse or

^{a)}On one-year sabbatical leave as Royal Society Kan Tong Po Visiting Professor in the City University of Hong Kong.

^{b)}Author to whom correspondence should be addressed; electronic mail: paul.chu@cityu.edu.hk

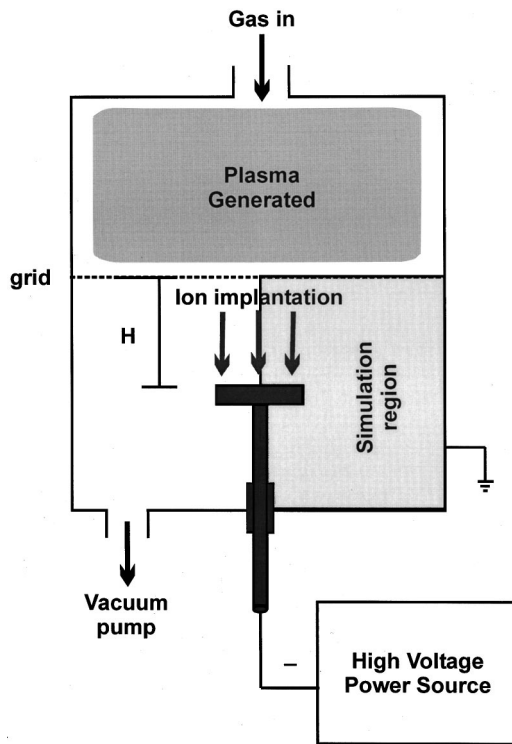


FIG. 1. Schematic diagram of the steady state dc setup for plasma implantation of semiconductor wafers. A grounded conducting grid is positioned above the wafer in the vacuum chamber. The simulation region and distance between the grid and wafer stage surface H are shown.

work in the steady state dc mode, the plasma density must be increased to reduce the sheath thickness. In other words, a high power and high efficiency plasma discharge is required, but there are a number of technical difficulties making such a system unrealistic at low pressure that is needed for monoenergetic implantation (i.e., ion mean free path is larger than the sheath thickness). An alternative is to operate at relatively high pressure around 2–3 mTorr. However, the chances of high voltage breakdown will increase and ion collisions will be more frequent, giving rise to a large number of low energy ions. Moreover, at high gas pressure, the surface oxidation rate will increase, such as in the oxygen PIII process to form SIMOX.

In this article, we present a novel concept to implant ions in the low pressure, steady state dc mode by introducing a grounded conducting grid on top of the wafer stage as illustrated in Fig. 1. The conducting grid, made of a compatible material to avoid contamination (e.g., a silicon coated mesh for implanting silicon wafers), divides the chamber into two parts. In the lower part, a strong electric field is formed between the negatively biased wafer stage and the boundaries created by the grid and the lower part of the chamber walls. The upper part confines the plasma since the grounded grid stops the expansion of the ion sheath from the bottom. In this way, a continuous low-pressure discharge can be maintained in the volume above the grid. Positive ions diffuse into the lower part through the grid and are implanted into the wafer. By performing particle-in-cell numerical simulation,¹² it can be observed that the ion paths do not depend on the applied voltage and ion mass. It is, however, sensitive to the initial

diffusion velocity and the relative size and placement of the chamber and wafer stage.

II. MODELING AND SIMULATION

The potential above the grid is at plasma voltage, whereas the potential of the part below the grid is influenced by the wafer stage applied voltage and can be solved by Laplace's equation in cylindrical coordinates:

$$\frac{\partial^2 \phi}{\partial r^2} + \frac{1}{r} \frac{\partial \phi}{\partial r} + \frac{\partial^2 \phi}{\partial z^2} = 0, \quad (1)$$

where ϕ is the potential, r is the radial distance from the center, and z is the longitudinal distance. It is assumed that the space charge density is approximately equal to zero in the lower part during the dc mode. In the ideal situation, the electric field is built up before the generation of the plasma. That is, there is initially no plasma inside the lower part. The secondary electrons created during the implantation are immediately absorbed by the chamber walls and grounded grid as they are light and energetic. The diffusion rate relative to the electric field strength is too small to gather the ions and change the potential. Equation (1) can be solved by the finite difference method.¹² We initially rest a sheet of particles/ions just below the grid in the simulation region shown in Fig. 1. The lower part of the chamber has a cylindrical symmetry and the simulation region can be reduced to a plane shown in Fig. 1. The particles will be pulled by the electric field and their trajectories are followed until they hit the wafer stage. The motions of the ions are governed by Newton's equations of motion in cylindrical coordinates¹²

$$v_i^r(f) = v_i^r(I) - \frac{q}{M} \frac{\partial \phi}{\partial r} t, \quad (2a)$$

$$v_i^z(f) = v_i^z(I) - \frac{q}{M} \frac{\partial \phi}{\partial z} t, \quad (2b)$$

$$\Delta r = v_i^r(I) t - \frac{1}{2} \frac{q}{M} \frac{\partial \phi}{\partial r} t^2, \quad (3a)$$

$$\Delta z = v_i^z(I) t - \frac{1}{2} \frac{q}{M} \frac{\partial \phi}{\partial z} t^2, \quad (3b)$$

where M is the ion mass, q is the ion charge, and $v_i^r(f)$, $v_i^r(I)$, $v_i^z(f)$, and $v_i^z(I)$ are the initial and final velocities of the ion at time step t , respectively. The internal dimensions are based on the semiconductor PIII instrument at the City University of Hong Kong.¹ The wafer stage, 0.056 m in thickness and 0.081 m in radius, is supported by a thin metal rod 0.3 m in length and 0.004 m in radius connected to the high power voltage supply. The vacuum chamber radius is 0.381 m, and the distance between the top of the wafer stage and the grid H can be varied.

III. RESULTS AND DISCUSSION

Our simulation shows that the ion paths will not change with the negative voltage applied to the wafer stage, mass, and charge states of the ions, provided that their initial velocity is small compared to the electric field strength. The ion

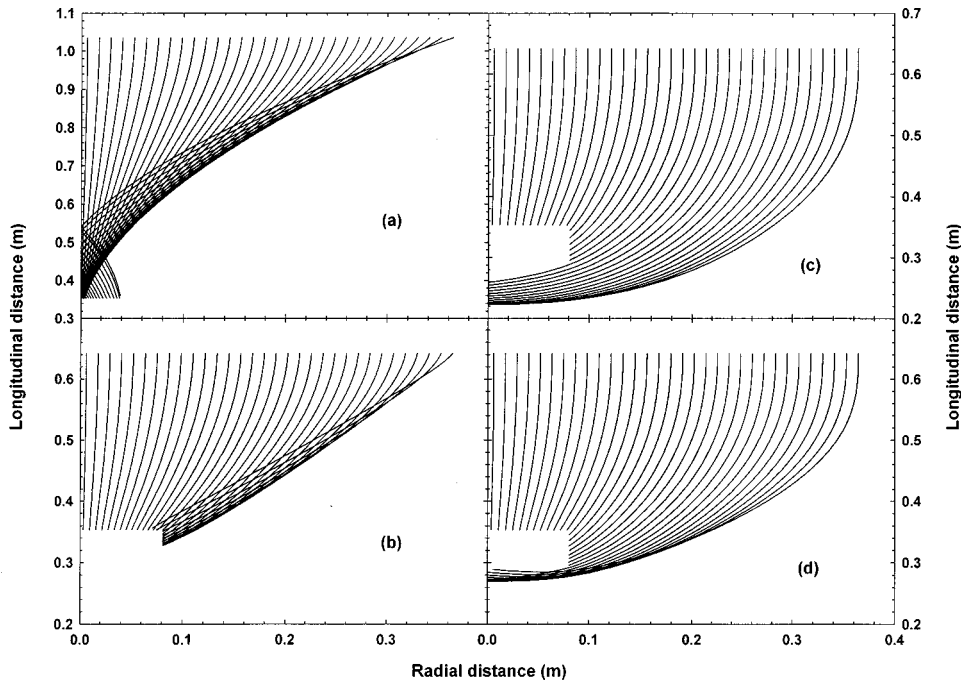


FIG. 2. The ion paths of the oxygen ions implanting from the grid to the wafer stage at -70 kV bias voltage: (a) the distance between the grid and wafer stage surface $H=70$ cm showing that the ions focus onto the center of the wafer; (b) $H=30$ cm showing that the whole wafer is implanted; (c) an initial downward drift velocity equivalent to 5×10^3 eV energy is applied to the ions and the ion trajectories are changed; (d) O^{2+} ions with the same downward drift velocity as (c) are used in the simulation and the ion paths become dependent on the charge state at the high initial velocity of the ions.

path of O^+ particles at $H=70$ cm and $H=30$ cm are depicted in Figs. 2(a) and 2(b). The applied voltage is -70 kV and the initial velocity of the particles is zero. Figure 2(a) reveals that some of the particles will pass through the mid-plane and become implanted at the other half of the wafer stage. At $H=70$ cm, the ions will focus onto the center of the wafer stage. The ion path is determined by the velocity vector, which in turn changes with the acceleration vector created by the force field in space. As shown in Eq. (2), the acceleration vector can be written as

$$\mathbf{a} = \left(-\frac{q}{M} \frac{\partial \phi}{\partial r} \right) \hat{r} + \left(-\frac{q}{M} \frac{\partial \phi}{\partial z} \right) \hat{k}. \quad (4)$$

The directional angle θ of the vector \mathbf{a} is

$$\theta = \tan^{-1} \left(-\frac{q}{M} \frac{\partial \phi}{\partial z} \bigg/ -\frac{q}{M} \frac{\partial \phi}{\partial r} \right) = \tan^{-1} \left(\frac{\partial \phi}{\partial z} \bigg/ \frac{\partial \phi}{\partial r} \right). \quad (5a)$$

It shows that the directional angle does not depend on the charge state and mass of the ions. The ratio of the partial differential of the scalar potential ϕ along the radial and longitudinal directions remains constant for different values of ϕ . It follows that the directional angle θ of the accelerating force field is totally determined by the local field structure of the lower part of the chamber. Therefore, if the ions are placed at the same starting position with zero initial velocity, they will pass through the same local field path. The amplitude A of the acceleration indeed will vary with the charge state, ion mass, and applied voltage

$$A = \frac{q}{M} \sqrt{\left(\frac{\partial \phi}{\partial r} \right)^2 + \left(\frac{\partial \phi}{\partial z} \right)^2}. \quad (5b)$$

Hence, by varying the charge state of the ion and applied voltage, the impact energy can be altered, and by varying the ion mass, the final velocity of the ion will be changed. How-

ever, if the ions have a large initial drift velocity compared to the maximum velocity created by the applied voltage, they will pass through a different local field structure. In this situation, the ion paths will vary with the charge state, ion mass, and applied voltage. The ion paths of the O^+ and O^{2+} particles with initial downward drift velocity 2.4468×10^5 m/s (equal to 5 keV impact energy of oxygen ions) are displayed in Figs. 2(c) and 2(d) for $H=30$ cm and applied voltage $= -70$ kV. Part of the ions have passed through the wafer stage and are implanted into the supporting rod.

Usually, in PIII, the ions are at room temperature, i.e., 0.026 eV, and the drift velocity is very small compared with the applied voltage. The working gas pressure is less than 1 mTorr and the gas is weakly ionized. The pressure gradient is small. Therefore, the ion path of different ions is similar.

The dose and energy uniformity along the implanted wafer are important issues for PIII in semiconductor applications. Here, we compare conventional PIII to our new dc method. As mentioned before, in PIII, there are a large number of low impact energy ions introduced into the wafer during the rise and fall times of each negative voltage pulse.¹¹ On the other hand, in the dc mode, the ion impact energy is constant since the ions are accelerated directly from the grid to the wafer stage. The uniformity of the ion dose on the wafer depends on two factors: the uniformity of the incident ion current and impact angle. Previous studies¹³ have shown that the PIII ion dose is higher at the edge of the wafer stage when the impact angle is off normal up to 45° . Therefore, although the depth profile is shallower at the edge, the ion dose is higher.¹³ In our dc mode, the implantation area is totally determined by the ratio of the radius of wafer stage r , the radius of the vacuum chamber R , the distance between the wafer stage and grid H , and thickness of the wafer stage D . The projected area from the grid to the wafer stage determines the incident dose into the wafer. Actually, the

smaller H is, the closer the ratio of the projected area to the implanted area to 1 and the better the incident dose uniformity. However, the shorter the distance between the anode (grid) and cathode (wafer stage), the higher the electric field that may lead to breakdown at high implantation voltage. The impact angle at the edge can be made normal by changing the thickness of the wafer stage. A thicker wafer stage can smooth out the electric field at the edge. In PIII, the ions are accelerated from the ion sheath and the impact angle is dominated by the spherical shape of the ion sheath. Our results show that the retained dose and impact energy in the dc mode can be made much more uniform by choosing the suitable internal dimensions of the lower part. Our simulation suggests that the best ratio is $r:R:H:D=1:4:2.5:2$. That is, a disk shaped chamber instead of the conventional cylindrical chamber is preferred. Our preliminary experimental data confirm it. We are in the process of collecting more experimental data that we will present in the near future.

IV. CONCLUSION

In summary, we have presented a novel technique to perform plasma implantation in a low gas pressure, steady state dc mode by introducing a grounded conducting grid on top of the wafer stage. The proposed method is similar to the conventional broad-beam beam-line approach to the limit that the target is located immediately in front of the extractor and substituting for the final extractor grid (and also grounding the plasma rather than the substrate). Hence, this method is in some sense similar to a modified beam-line method or a modified plasma source ion implantation method, and can be envisaged to be lying between the two. However, in our process, the ion beam is not filtered according to the ion mass-to-charge ratio, and the throughput is much higher than conventional beam-line ion implantation provided that there is sufficient control on the plasma species.

Our simulation results reveal that the ions diffusing through the grid are implanted into the wafer stage with standard trajectories. These ion paths will not change with the negative voltage applied to the wafer stage, ion mass, and charge state of the ions, provided that their initial velocity is small compared to the electric field. This is because the directional angle of the acceleration vector does not depend on the mass and charge state of the ions, and the ratio of the

partial differential of the scalar potential ϕ along the radial to that in the longitudinal direction remains constant for different applied voltages. The ion dose and impact energy uniformity is totally determined by the internal ratio between the radius of wafer stage r , the radius of chamber R , the height between the wafer stage and the grid H , and the thickness of the wafer stage D . Our results suggest an optimal ratio of $r:R:H:D=1:4:2.5:2$. Besides retaining the high throughput and parallel processing advantages of PIII, the implantation energy in this dc mode can be extended far beyond the limit of PIII as the technique obviates the use of the power modulator, which not only limits the implantation energy but also is the most expensive and technological complex hardware component in a PIII system.

ACKNOWLEDGMENTS

The work was supported by City University of Hong Kong Strategic Research Grant No. 7000964 and Hong Kong Research Grants Council Earmarked Grant Nos. 9040344 and 9040412. The authors also acknowledge the Royal Society Kan Tong Po Visiting Professor Fellowship.

- ¹P. K. Chu, S. Qin, C. Chan, N. W. Cheung, and L. A. Larson, *Mater. Sci. Eng.*, **R. 17**, 207 (1996).
- ²G. A. Collins, R. Hutchings, K. T. Short, J. Tendys, X. Li, and M. Samandi, *Surf. Coat. Technol.* **74–75**, 417 (1995).
- ³K. Komvopoulos, B. Wei, S. Anders, A. Anders, and I. G. Brown, *J. Appl. Phys.* **76**, 1656 (1994).
- ⁴Z. M. Zeng, B. Y. Tang, P. K. Chu, X. B. Tian, S. Y. Wang, and X. F. Wang, *J. Vac. Sci. Technol. B* **17**, 851 (1999).
- ⁵X. C. Zeng, T. K. Kwok, A. G. Liu, P. K. Chu, and B. Y. Tang, *J. Appl. Phys.* **83**, 44 (1998).
- ⁶S. Y. Wang, P. K. Chu, B. Y. Tang, J. C. Yan, and X. C. Zeng, *Surf. Coat. Technol.* **98**, 897 (1998).
- ⁷Z. M. Zeng, T. K. Kwok, X. B. Tian, B. Y. Tang, and P. K. Chu, *J. Appl. Phys.* **86**, 120 (1999).
- ⁸P. K. Chu, X. Lu, S. S. K. Iyer, and N. W. Cheung, *Solid State Technol.* **40**, S9 (1997).
- ⁹X. Lu, S. S. K. Iyer, J. Lee, B. Doyle, Z. N. Fan, P. K. Chu, C. M. Hu, and N. W. Cheung, *J. Electron. Mater.* **27**, 1059 (1998).
- ¹⁰X. B. Tian, B. Y. Tang, and P. K. Chu, *J. Appl. Phys.* **86**, 3567 (1999).
- ¹¹Z. N. Fan, Q. C. Chen, P. K. Chu, and C. Chan, *IEEE Trans. Plasma Sci.* **26**, 1661 (1998).
- ¹²D. T. K. Kwok, P. K. Chu, and C. Chan, *IEEE Trans. Plasma Sci.* **26**, 1669 (1998).
- ¹³D. T. K. Kwok, P. K. Chu, B. P. Wood, and C. Chan, *J. Appl. Phys.* **86**, 1817 (1999).