TWO STEP O_2/N_2O PLASMA ANNEALING FOR THE REDUCTION OF LEAKAGE CURRENT IN AMORPHOUS Ta_2O_5 FILMS

W.S. LAU,* M.T. CHANDIMA PERERA,** T. HAN,*** N. P. SANDLER,*** C.H. TUNG,** T.T. SHENG,** P.K. CHU, **** and T.C. CHONG*****
*Chartered Semiconductor Manufacturing Ltd., R&D Advanced Technology Department, 60 Woodlands Industrial Park D St.2, Singapore 738406, Republic of Singapore.
E-mail: lauws@csm.st.com.sg
** Institute of Microelectronics, 11 Science Park Road, Singapore Science Park II, Singapore 117685, Republic of Singapore
***Lam Research Corporation, 4650 Cushing Parkway, Fremont, California 94538, USA
****Department of Physics and Materials Science, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong
*****Data Storage Institute, National University of Singapore, 10 Kent Ridge Crescent, Singapore 119260, Republic of Singapore

ABSTRACT

As deposited tantalum pentoxide (Ta_2O_5) films are amorphous. The films will remain amorphous after O_2 or N_2O plasma annealing at low temperature. High temperature annealing will produce polycrystalline films where grain boundaries can generate leakage current. Previously, we have shown that N_2O plasma annealing is superior to O_2 plasma annealing in terms of leakage current reduction for Al/Ta_2O_5/Si capacitors. However, for TiN/Ta_2O_5/Si capacitors, the leakage current tends to be higher at low bias voltage for N_2O plasma annealing compared to O_2 plasma annealing. By adding an O_2 plasma annealing step and then comparing TiN/Ta_2O_5/Si capacitors with two step O_2/N_2O plasma annealing with respect to similar structures with two step O_2/O_2 plasma annealing , it can be easily seen that TiN/Ta_2O_5/Si capacitors with two step O_2/N_2O plasma annealing have lower leakage current compared to similar structures with two step O_2/O_2 plasma annealing throughtout the voltage range tested.

INTRODUCTION

Tantalum pentoxide (Ta_2O_5) films, which have a dielectric constant of 20-25 as compared to a dielectric constant of 3.9 for SiO_2 or 7 for Si_3N_4, have demonstrated promise as a dielectric for charge storage in 1 Gb DRAMs [1]. However, Ta_2O_5 tends to leak much more than SiO_2 or Si_3N_4. Quite frequently, a post-deposition annealing in an oxidising ambient is needed to reduce the leakage current. Sun and Chen [2]-[4] demonstrated that Ta_2O_5 films treated by N_2O rapid thermal annealing (RTA) are much less leaky than those treated by conventional O_2 RTA at an annealing temperature of about 800°C. We have confirmed these findings [5]-[6]. We have also explained the superiority of N_2O compared to O_2 by the lower energy required to break the nitrogen-oxygen bond in a N_2O molecule compared to the energy required to break the O=O bond in an O_2 molecule [7]. Recently, Sun and Chen demonstrated that N_2O furnace annealing is also superior to O_2 furnace annealing [8]. We expect that this finding can also be explained by the same theory. One important mechanism of leakage current is related to grain boundaries. High temperature annealing tends to cause the as deposited amorphous Ta_2O_5 film to crystallize into a polycrystalline film, resulting in leakage current due to grain boundaries. For example, Aoyama et al. observed that their polycrystalline Ta_2O_5 film after annealing at 700°C was more leaky than their amorphous Ta_2O_5 film after annealing at 650°C [9]. Hence, there is a demand to develop a method of annealing at lower temperature in order to make the leakage current even lower. In 1992, Park et

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al. demonstrated that a N_2O plasma annealing is superior to high temperature O_2 annealing for the reduction of leakage current of Ta_2O_5 films [10]. Subsequently in 1994, Kamiyama et al. demonstrated that low temperature O_2 plasma annealing is superior to high temperature O_2 annealing [11]. No comparison between N_2O plasma annealing and O_2 plasma annealing has been made by Park et al. [10] and Kamiyama et al. [11]. In 1998, we demonstrated that low temperature N_2O plasma annealing is also superior to low temperature O_2 plasma annealing in the reduction of leakage current in Ta_2O_5 films with the help of Al/Ta_2O_5/Si capacitors [12]. For practical application, it is well known that TiN is the better electrode material compared to Al [13]. We have also been working on the application of low temperature N_2O plasma annealing and also low temperature O_2 plasma annealing to TiN/Ta_2O_5/Si capacitors. As discussed below in this paper, we found that TiN/Ta_2O_5/Si capacitor with one step N_2O plasma annealing tends to have larger leakage current than a similar structure with one step O_2 plasma annealing at low bias voltage.

In this paper, we will demonstrate that N_2O plasma annealing is also superior to O_2 plasma annealing in the reduction of leakage current in Ta_2O_5 films for the whole bias range if we put one extra step of O_2 plasma annealing before the N_2O plasma annealing. If we make a comparision between TiN/Ta_2O_5/Si capacitor with two step O_2/N_2O plasma annealing and TiN/Ta_2O_5/Si capacitor with two step O_2/O_2 plasma annealing, it can easily seen that the former has lower leakage current for the whole bias range investigated by us..

Previously, we have demonstrated that defect states in Ta_2O_5 can be detected by a novel zero-bias thermally stimulated current (ZBTSC) technique and the leakage current can be reduced by the reduction of defect states detected by ZBTSC [14]-[15]. A correlation with the defect state density has also been successfully made for two step N_2O plasma and O_2 plasma annealed samples.

EXPERIMENT

Ta_2O_5 films were deposited onto n^+-Si wafers by low-pressure metal-organic chemical vapour deposition (LPMOCVD) in a Lam Research DSM9800 system as reported before [16]. For this study, the film thickness was about 15 nm. The samples were annealed by O_2 or N_2O plasma annealing at 350°C for 30 min. The plasma annealing was performed in a commercial PECVD (plasma enhanced chemical vapour deposition) chamber. The pressure was 0.45 Torr. The RF (13.56 MHz) power used was 100 W. TiN was sputtered onto Ta_2O_5 films. Au/Cr (100/30 nm) dots with a diameter of 1 mm were evaporated through a shadow mask onto Ta_2O_5 inside an electron beam evaporator. With Au/Cr dots serving as mask, the extra TiN was etched off with a NH_4OH:H_2O_2:H_2O (1:1:5) solution. With the top side covered by photoresist, the Ta_2O_5 film deposited on the backside of the wafer during the LPMOCVD process was then removed by chemical etching and Al was evaporated to form a back contact. The photoresist on the topside was removed. A post-metallization annealing at 400°C was performed in a furnace tube for 5 min. in pure nitrogen. Please note that previously we used a post-metallization annealing at 400°C for 30 min in nitrogen to reduce the leakage current of relatively thick Ta_2O_5 films with a thickness of about 100 nm [14]. For relatively thin Ta_2O_5 films with a thickness of about 15 nm, the annealing time has to be reduced to only 5 min., as discussed by us before [12]. The leakage current will be significantly higher for a longer annealing time. The defect states in the samples were characterized by the zero-bias thermally stimulated current (ZBTSC) technique developed by us before [14]-[15].

As discussed in our previous work, the interfacial SiO_x layer between Ta_2O_5 and Si is important because it can lower the capacitance of the Ta_2O_5 capacitor. Previously, we discussed about a film observed on top of the Ta_2O_5 film with O_2 plasma annealing with the help of cross-sectional transmission electron microscopy (XTEM) [12]. We pointed out that this film is a SiO_x

film which has also been observed by another research group [17]-[19]. Both the interfacial SiO_x layer between Ta_2O_5 and Si and the top SiO_x film will have significant effect on the capacitance of the samples. Both XTEM and capacitance-voltage (C-V) measurements were done to investigate these effects. C-V measurements were usually done at 1 kHz to avoid series resistance effects.

RESULTS AND DISCUSSION

As shown in Fig. 1, the TiN/ Ta_2O_5/Si capacitor with N_2O plasma annealing without post-metallization annealing has lower leakage than the TiN/ Ta_2O_5/Si capacitor with O_2 plasma annealing without post-metallization annealing for a bias voltage higher than 0.6V; however, when the bias voltage is lower than 0.6V, the former gives a higher leakage current. Similarly, also as shown in Fig. 1, the TiN/ Ta_2O_5/Si capacitor with N_2O plasma annealing and post-metallization annealing has lower leakage than the TiN/ Ta_2O_5/Si capacitor with O_2 plasma annealing and post-metallization annealing for a bias voltage higher than 0.6V; however, when the bias voltage is lower than 0.6V, the former gives a higher leakage current. This is the case for one step plasma annealing. As discussed by us before [12], single step O_2 plasma annealing can create a thin SiO_x layer on top of the Ta_2O_5 film whereas single step N_2O plasma annealing cannot. We suspect that the TiN deposition process may cause some damage to the Ta_2O_5 film when there is no SiO_x layer on top of the Ta_2O_5 film. Hence, we experimented with a two step O_2/N_2O plasma annealing; the purpose of the first step O_2 plasma annealing was to create a SiO_x layer on top of the Ta_2O_5 film. The presence of this layer can be verified by XTEM. As shown in Fig. 2, TiN/ Ta_2O_5/Si capacitor with two step O_2/N_2O plasma annealing has lower leakage than the TiN/ Ta_2O_5/Si capacitor with two step O_2 /O_2 plasma annealing for the whole range of bias voltage used. This is the case for samples with and without post-metallization annealing.

As shown in Fig. 3, the ZBTSC spectra clearly showed that the sample with two step O_2/N_2O plasma annealing has less defect B, which is related to Si contamination, compared to the sample with two step O_2 /O_2 plasma annealing. This is similar to our previous observations [12].

As shown in Fig. 4, the C-V characteristics showed that the sample with two step O_2/N_2O plasma annealing has higher capacitance compared to the sample with two step O_2 /O_2 plasma annealing. This can be easily explained as follows: The two step O_2 /O_2 plasma annealing created a thicker SiO_x layer on top of the Ta_2O_5 film. This explanation can be easily confirmed by XTEM. As shown in Fig. 5a and 5b, the SiO_x layer on top of the Ta_2O_5 film is thinner for the sample with two step O_2/N_2O plasma annealing compared to the sample with two step O_2 /O_2 plasma annealing. This can also be seen by the thicknesses of the top and bottom SiO_x layers shown in Table I for two samples with a Ta_2O_5 film (15 nm) on Si.

CONCLUSION

Two step O_2/N_2O plasma annealed samples showed consistently better leakage current characteristics than one step N_2O annealed samples or two step O_2/O_2 annealed samples for TiN/Ta_2O_5/Si capacitors.

Table I Thickness of top and bottom SiO_x layers after two step plasma annealing

Process condition	Thickness of bottom SiO_x (nm)	Thickness of top SiO_x (nm)
O_2/N_2O plasma annealing	~ 2.2	~3.3
O_2/O_2 plasma annealing	~ 2.2	~5.5

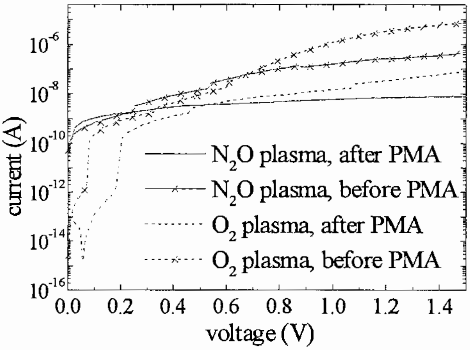

Fig. 1. The I-V characteristics of $Au/Cr/TiN/Ta_2O_5/n^+$-Si with O_2 plasma before post metalization annealing (broken line with cross), with N_2O plasma before post metalization annealing (solid line with cross), with O_2 plasma after post metalization annealing (broken line), and with N_2O plasma after post metalization annealing (solid line). The polarity of the applied voltage was positive for the top Au/Cr/TiN contact.

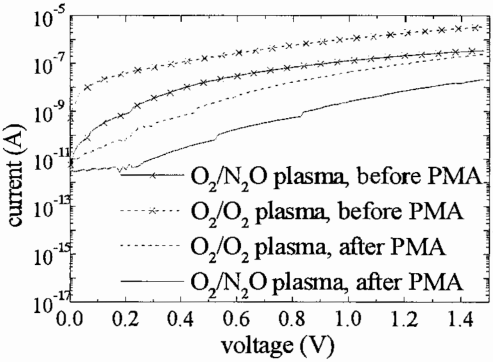

Fig. 2. The I-V characteristics of $Au/Cr/TiN/Ta_2O_5/n^+$-Si with two step O_2/O_2 plasma annealing before post metalization annealing (broken line with cross), with two step O_2/N_2O plasma before post metalization annealing (solid line with cross), with two step O_2/O_2 plasma after post metalization annealing (broken line), and with two step O_2/N_2O plasma after post metalization annealing (solid line). The polarity of the applied voltage was positive for the top Au/Cr/TiN contact.

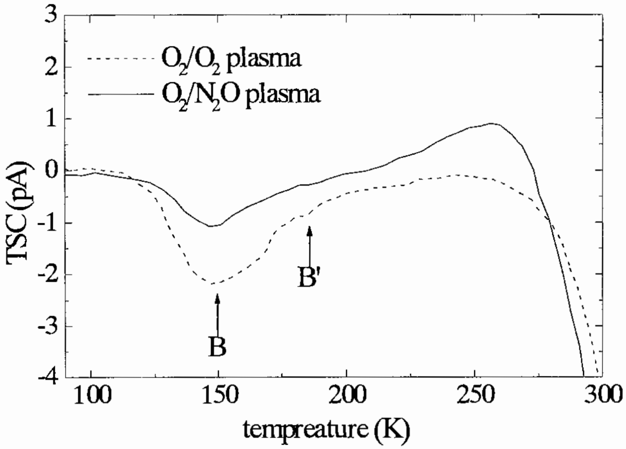

Fig. 3. The ZBTSC spectra of Au/Cr/TiN/Ta$_2$O$_5$/n$^+$-Si with O$_2$/O$_2$ plasma annealing (broken line) and O$_2$/N$_2$O plasma annealing (solid line). A post-metallization annealing at 400°C was performed in a furnace tube for 5 min. in pure nitrogen.

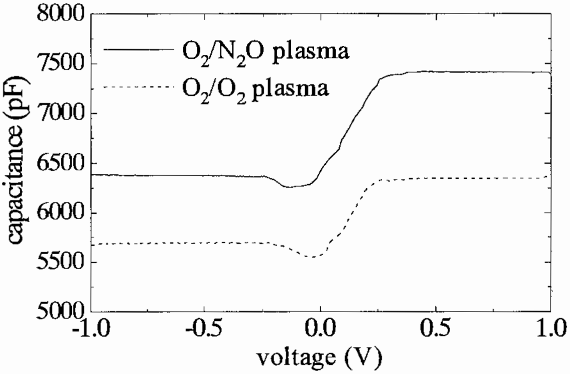

Fig. 4. The C-V characteristics of Au/Cr/TiN/Ta$_2$O$_5$/n$^+$-Si with O$_2$/O$_2$ plasma annealing (broken line) and O$_2$/N$_2$O plasma annealing (solid line). A post-metallization annealing at 400°C was performed in a furnace tube for 5 min. in pure nitrogen.

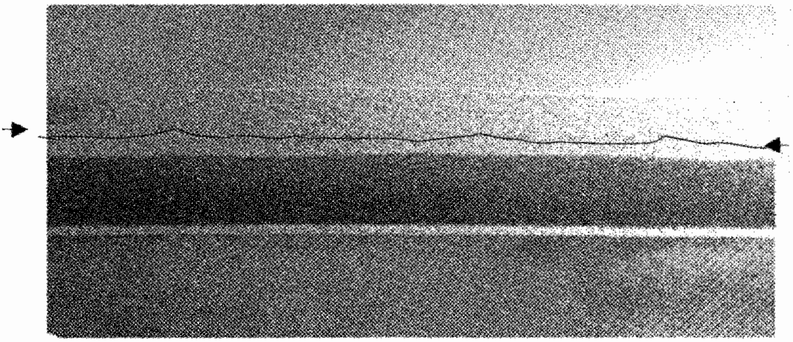

Fig. 5a XTEM micrograph for Ta_2O_5/Si with two step O_2/N_2O plasma annealing. The thickness of the Ta_2O_5 film is about 15 nm. The SiO_x layer on top of Ta_2O_5 is marked by arrows.

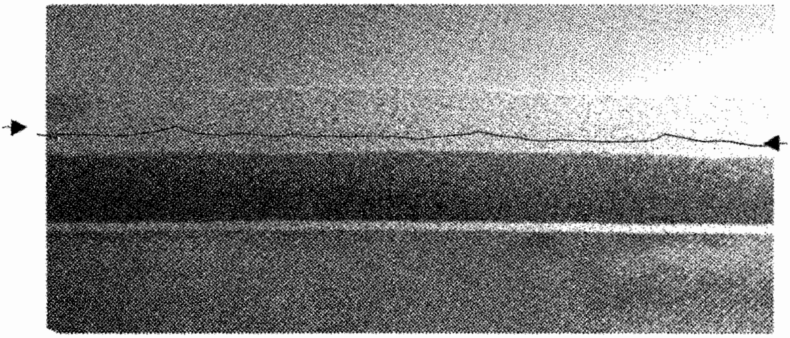

Fig. 5b XTEM micrograph for Ta_2O_5/Si with two step O_2/ O_2 plasma annealing. The thickness of the Ta_2O_5 film is about 15 nm. The SiO_x layer on top of Ta_2O_5 is marked by arrows.

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