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TWO DIMENSIONAL PARTICLE-IN-CELL SIMULATION OF PLASMA IMMERSION ION IMPLANTATION INTO PLANAR WAFER

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Plasma immersion ion implantation (PIII) is a burgeoning technique for semiconductor processing due to its high dose rate and simple instrumentation [1-4]. In PIII, the wafers are surrounded by high-density plasma and pulse-biased to a high negative potential relative to the chamber wall. Ions generated in the plasma shroud are accelerated across the sheath formed around the samples and implanted into the surface of the targets. Since the entire wafer is implanted simultaneously, the implantation time is much shorter than that of conventional beamline techniques and the time advantage is more substantial for larger wafer size such as 300 mm. It has thus been used to form shallow junctions [5-8], synthesize silicon-on-insulator (SOI) structures [9-17], process flat panel display materials [18], and so on.

Most PIII instruments consist of a stainless steel cylindrical vacuum chamber with internal liners made of aluminum or compatible materials to minimize contamination to the specimens. The sample holder (chuck) is typically made of stainless steel (for high temperature and general applications) or aluminum (for low temperature processing) and is typically located in the center of the chamber. We have recently discovered that the sample stage (chuck) design can impact ion uniformity significantly. Using a two dimensional particle-in-cell numerical model, we have investigated three different chuck designs and conclude that insulators on the stage can alter the adjacent electric field and ion trajectories. Even though the conventional stage design incorporating a quartz shroud reduces the load on the power supply and contamination, it yields ion dose and energy non-uniformity unacceptable to the semiconductor industry. Thus, for semiconductor applications, the stage should be made of a conductor, preferably silicon or silicon coated materials and free of quartz.

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