

PART ONE OF TWO

## Plasma doping: Progress and potential

**P.K. Chu**, City University of Hong Kong, **S.B. Felch**, Varian Semiconductor Equipment Assoc., Palo Alto, California, **P. Kellerman**, **F. Sinclair**, Eaton Corp., Beverly, Massachusetts, **L.A. Larson**, SEMATECH, Austin, Texas, **B. Mizuno**, Matsushita Electric Industrial Co. Ltd., Moriguchi, Osaka, Japan

Beam-line ion implantation, the pre-eminent doping method in silicon, is being pushed to the limit by the need to fabricate ultra-shallow junctions. Plasma doping is envisaged to be the alternative technique suited for the shift to simpler, more economical, higher throughput, and cluster-compatible hardware. The technology has gained much momentum in the past several years and an international plasma doping users group has been formed to bring together equipment manufacturers, process engineers, and researchers. In this article (part one of two parts), we will review the current status of plasma doping, present the latest device data, and discuss process and equipment issues.

Ultra-shallow junctions are required for deep sub-micrometer integrated circuits in the 21st century. The most logical fabrication method is to extend the beam-line ion implantation technology to ultra-low energies. Even though low-energy beam-line ion implantation has been demonstrated [1-3], it suffers from slow throughput.

Several alternative techniques have been proposed, including plasma doping (PD) [4-11], high-temperature rapid vapor doping (RVD) [12, 13], room-temperature vapor doping [14], and gas immersion laser doping (GILD) [15, 16]. Plasma implantation methods — PD, plasma assisted doping (PLAD), and plasma immersion ion implantation (PIII) — have been regarded as the most promising candidates to obtain ultra-shallow doping profiles due to low implantation energy, high throughput, low machine cost, room temperature operation, and compatibility to a CMOS production environment.

When the 1997 National Technology Roadmap for Semiconductors was issued, PD was clearly listed as the leading candidate among several for the alternative doping method to compete with low-energy beam-line ion implantation (II). Here we describe the current status of PD, process and equipment issues, and the outlook of PD as a replacement for beam-line ion implantation in the fabrication of ultra-shallow junctions.

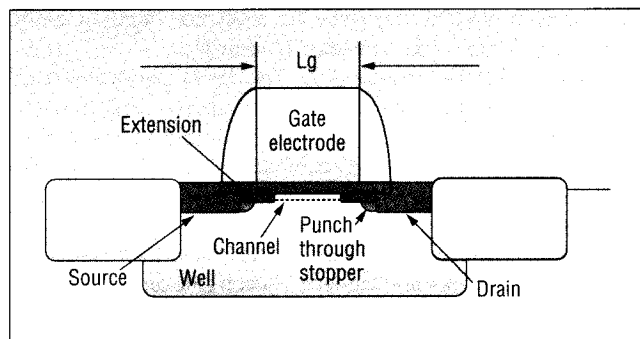


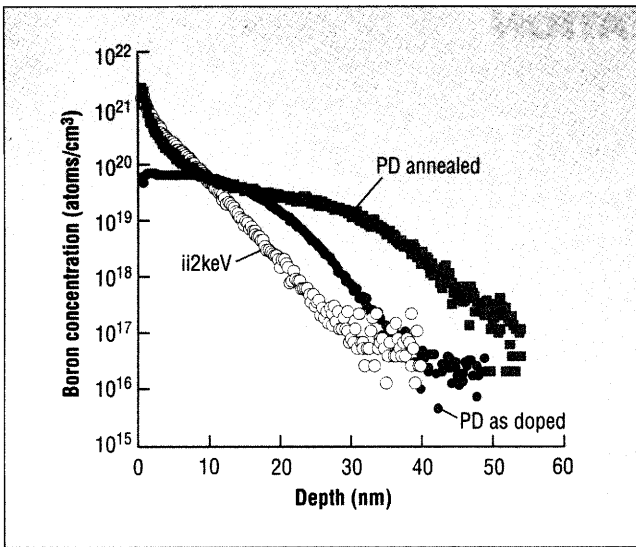
Figure 1. Cross section schematic of the 0.17µm PMOSFET.

### Ultra-shallow junction formation by PD

PD can be implemented in three different configurations: gas source PD, solid source PD (SPD), and RVD with plasma pre-treatment. SPD is gaining popularity as the use of toxic dopant gases can be eliminated. Gas source PD is usually performed in a  $B_2H_6$  plasma diluted by He sustained by an electron cyclotron (ECR) or radio frequency (RF) plasma source. The aim of dilution is to control the implantation rate and toxic dopant species. The wafer is attached to a sample holder or chuck acting as the cathode. When a bias of several hundred volts is applied to the sample chuck, positive ions are implanted into the wafer at the applied voltage assuming a collisionless condition (plasma sheath thickness  $<$  ion mean free path). Contrary to beam-line ion implantation, the entire wafer is implanted simultaneously, and the implantation time is independent of the wafer dimension so cost does not go up with wafer size.

Figure 1 depicts the cross section of a device in which the source/drain extensions are formed by PD ( $0.5\% B_2H_6/He$ , 100 sec) and with low-energy ion implantation ( $5keV, BF_2, 6 \times 10^{13} cm^{-2}$ ) for the control. The gate electrodes and source/drain electrodes are also formed by PD ( $5\% B_2H_6/He$ , 100 sec) [5].

The SIMS (secondary ion mass spectrometry) depth profiles of the as-implanted ( $5\% B_2H_6/He$ , 100 sec) and annealed ( $1000^\circ C$ ,

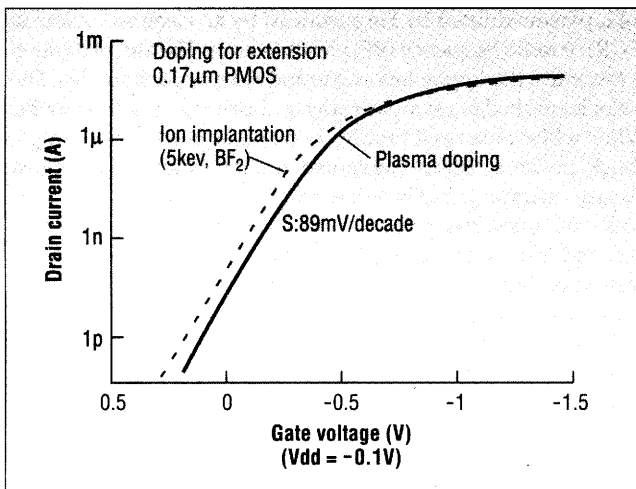


**Figure 2.** SIMS depth profiles of PD junction (as implanted, annealed) and a 2keV beam-line implant; ii-ion implant; PD=plasma doping.

10 sec) samples are shown in Fig. 2. For comparison, the boron depth profile of a 2keV as-implanted beam-line sample is overlaid. The PD profiles show a higher surface boron concentration compared to the beam-line profile due to surface chemisorption. The as-implanted PD profile has a junction depth of 25nm whereas it is 50nm for the annealed PD sample.

**Device characteristics and yield.** The device performance of PMOSFETs fabricated by industrial CMOS processes at both AMD and CNET using PD is excellent. AMD has found in general that PMOS devices fabricated by PD exhibit subthreshold swing, off-state leakage, and hot-carrier reliability similar to the beam-line ones. Also, higher drive currents are observed in the plasma-doped devices. These improvements can be attributed to the reduced source/drain resistance and higher inversion gate capacitance due to better activation with PD. CNET has found that the electrical results (especially the normalized ion for deep sub-micrometer PMOSFETs) are better than those obtained with standard BF<sub>2</sub><sup>+</sup> implantation. Other parameters improve due to the reduced lateral diffusion. Finally, the oxide reliability improves when the extensions are plasma doped.

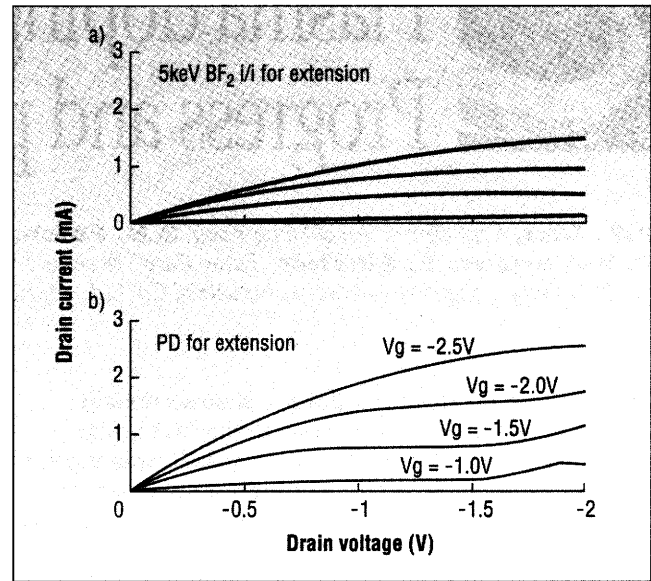
Another device study by Samsung [17] compares MOSFETs where the source/drain/gate and shallow source/drain



**Figure 3.** Subthreshold characteristics of 0.17µm PMOSFET fabricated by PD.

extension are fabricated by BF<sub>3</sub> PD with those formed employing BF<sub>2</sub> beam-line II. It is found that the gate oxide reliability, drain current, and transconductance of the PMOSFETs are remarkably improved. Cobalt salicide formation is also found to be compatible with plasma-doped source/drain junctions. Also, no evidence of plasma damage or fluorine-induced gate oxide reliability degradation has been detected in the PD samples.

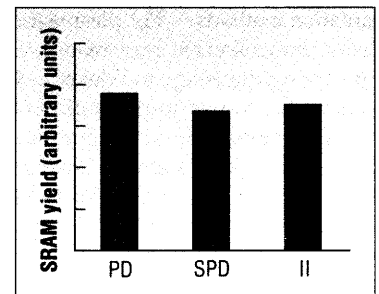
As an example, the subthreshold characteristics of the 0.17µm PMOS fabricated in Matsushita [5] are shown in Fig. 3. The subthreshold slope of 89mV/decade for the PD sample matches that of 5keV beam-line BF<sub>2</sub> implantation.



**Figure 4.** Comparison of I-V characteristics of a) beam-line doped and b) PD junctions.

The I-V characteristics shown in Fig. 4 are also excellent. The PD sample has higher drain current than the beam-line one, as demonstrated by the higher saturation currents. Recently, Samsung [17], Micron, French Telecom [18], AMD, Varian [19], and Matsushita [20] have demonstrated that plasma-doped MOSFETs show higher transconductance and carrier activation efficiency in sub-0.18µm devices. Trench doping for DRAM capacitor cells has also been shown by Siemens-IBM [18]. The yield of 256kb SRAM structures fabricated by PD and beam-line II has been compared. As shown in Fig. 5, the yields of gas source PD, SPD, and beam-line II are comparable [21].

**Throughput and surface metal contamination.** Aside from the low energy, the other significant advantage of PD is its high throughput. For beam-line II, the maximum beam current density for the whole wafer area is about 7µA/cm<sup>2</sup> (5mA boron beam at 3keV for a 300mm wafer). However, it is about 3mA/cm<sup>2</sup> for plasma doping. One can therefore expect a 400× improvement in the throughput in the 300mm wafer age.



**Figure 5.** Yield comparison among gas source plasma doping (PD), solid source plasma doping (SPD), and beam-line ion implantation (II).

continued on page 58

Plasma doping continued from page 56

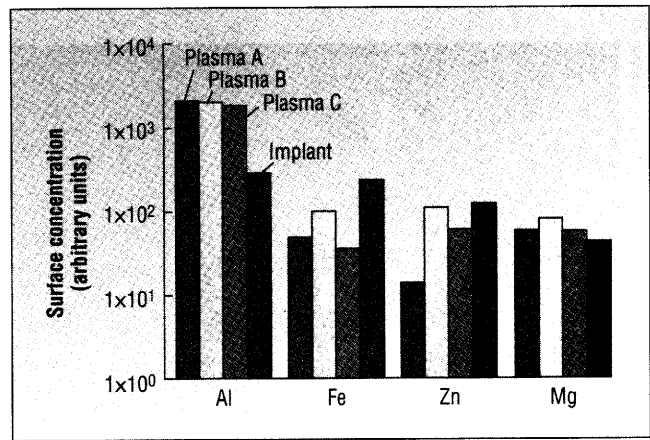
Figure 6 compares the surface metal contamination on PD and beam-line implanted samples. The surface Al, Fe, Zn, and Mg concentrations on the three PD samples are comparable to those on the beam-line implanted wafer [21], further illustrating the viability of PD. These and other process related issues will be discussed in more detail in the next section.

### Process-related issues

PD promises enormous productivity improvements so it is attractive to manufacturing managers, but adoption will be blocked unless it can demonstrate yield and consistent process control. Control implies both an ability to tailor the doping profile to fit a particular requirement derived from a device model (theoretical predictability) and the capability to execute the same process every day in a manufacturing environment (practical reproducibility).

**Theoretical predictability.** One of the great strengths of conventional beam-line II is its excellent theoretical predictability over a wide range of process conditions. Such an implanter has three principal controls: species, energy, and dose. Each of these parameters is mapped directly to the device physicists' models. The species selected by the mass analysis magnet defines the ratio of the atomic or molecular ion mass to its charge state over about two orders of magnitude. The energy is defined by the accelerating voltage over three orders of magnitude and can be used to calculate the doping profile according to models that have been under intensive development over the last three decades and are now very accurate for all but the most extreme energies. The dose maps directly to the concentration, allowing proportional control over six orders of magnitude.

Plasma doping has a long way to go before it can match beam-line II in terms of theoretical predictability. The as-implanted



**Figure 6.** Comparison of Al, Fe, Zn, Mg surface concentrations on three PD samples vs. a beam-line ion implanted sample.

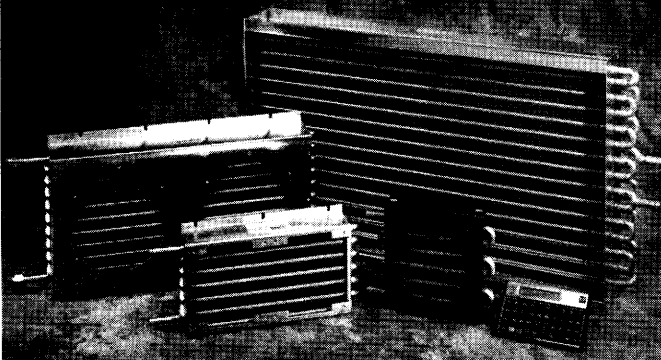
junction depth is primarily determined by the pulse voltage and has been shown to vary linearly with this voltage over a range from 0.14–5 kV [22]. However, in PD, all ionized species in the plasma are implanted. For example, with  $\text{BF}_3$  gas, the predominant ions implanted are  $\text{BF}_2^+$ ,  $\text{B}^+$ , and  $\text{F}^+$ . Furthermore, the energy spectrum of the ions contains components lower than the pulse voltage due to ions present in the sheath at the onset and turn off of the pulse, as well as because of the finite rise and fall times of the pulse. While low-energy ions are not detrimental (even preferred) in shallow junction formation, both of these factors can affect the dopant depth profile. They offer the process engineer new opportunities for tailoring this profile, being of particular use for shallow junctions [23–25]. PD has also been shown to satisfy the 1997 SIA National Technology Roadmap requirements at the 100nm node for source/drain extensions, where annealed junction depths must be <40nm and the activated surface dopant concentration must be above  $1 \times 10^{20}$  atoms/cm<sup>3</sup> [26].

Although PD's new multidimensional richness may offer process advantages, it also creates many challenges for the equipment manufacturer. Parameters typically monitored on PD tools at this time can only be indirectly mapped to process results. Plasma source parameters, such as pressure and power, can only be coupled to plasma ion fractions by complex models [27, 28]. The total current measured from the platen is only indirectly related to the ion current due to the presence of secondary electron and displacement currents (current needed to charge the platen to its pulsed voltage) [29]. Process engineers must resort to relating these machine controllable parameters directly to implant profiles (provided by SIMS measurements, for example), and then use models to interpolate between values. Clearly, more work is needed to improve the predictive capability in PD. Besides improving the models, further instrumentation may be required, such as Faraday cups, emission spectrophotometers, and ion mass spectrometers.

**Practical reproducibility.** Once a process engineer has defined the process that achieves the required sheet resistance,  $R_s$ , and junction depth,  $x_j$ , for the optimal device performance, attention shifts to repeating the process in routine manufacturing. The early stages of process qualification will often include small adjustments to the process control parameters to home in on specific device parameters. Thus, it is important that repeated runs under the same conditions produce results that have as small a variability as possible. In addition, it is critical that the relationships between tool parameter setting and device characteristics are continuous and well-behaved functions that allow rapid convergence on the

continued on page 60

# Heat Exchangers!



See us at SEMICON WEST, Booth #2972 South Hall

## LYTRON

Total Thermal Solutions

55 Dragon Court • Woburn, MA 01801

TEL 781-933-7300 • FAX 781-935-4529

www.lytron.com

ALSO AVAILABLE:

Chillers

Cold Plates

Cooling Systems



