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The effect of amorphous Si on the epitaxial growth of $CoSi_2$ by Co/Si/Ti/Si solid state epitaxy

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Abstract: An amorphous Si layer was added for the reduction of Si consumption in the ultra-shallow junctions during the silicide formation. The present experiments show an epitaxial $CoSi_2$ layer with good single-crystalline quality was grown by Co/ Si/ Ti /Si(100) reaction. By varying the thickness of interposed amorphous Si, its effect on the epitaxial $CoSi_2$ growth and self-aligned process was investigated. The film structure and crystallinity were characterized by X-ray diffraction (XRD), Rutherford backscattering(RBS) / channeling and transmission electron microscopy (TEM). RBS/C shows that the channeling yield minimum of $CoSi_2$ formed by Co(15nm) /Si(4nm) /Ti(3nm)/Si(100) reaction is 5.2%. It was also demonstrated that within a certain thickness range for the deposited Si, the self-aligned silicide (SALICIDE) contact structure can be formed by such a multilayer.

Introduction

As devices are scaled down to deep submicron dimension, formation of a uniform, thermally stable, low resistivity silicide contact to ultra shallow junctions is one of the key issues for device fabrication technology. Among all silicides, cobalt disilicide attracts special interest, not only because of its low resistivity (14 ~ 20 μΩ•cm) and high thermal stability, but also its excellent lattice match with Si, ~1.2% at RT.

Recently a new method of epitaxial growth of $CoSi_2$ on Si substrate has attracted much attention. This new $CoSi_2$ solid phase epitaxy(SPE) technique is based on the solid phase interaction of Co/Ti/Si ternary system and received intensive studies in the past few years[1-3]. It has been found that epitaxial $CoSi_2$ films with flat interface, high conductivity and high temperature stability can be grown on both Si(100) and Si(111) substrate by annealing a Co/Ti/Si structure. There is also an effort to develop a self-aligned process by this method which can be applied to improve the present fabrication technology of ULSI. Generally, it has been believed that the success of this epitaxial growth is due to the reducing nature of Ti on the native oxide of the Si substrate and to the fact that the interdiffusion of Co and Si is slowed down by the Ti-induced barrier layer, which favors epitaxial nucleation and growth of $CoSi_2$.[4-5].

As the device dimension is scaled down to deep submicron range, the problem of consumption of Si in shallow junction during the formation of silicide is more and more serious. 1nm Co will consume 3.6nm Si to form 3.5nm $CoSi_2$ film. The consumption of excessive Si in shallow junction will result in degradation of electrical characteristic of pn-junction. So it is important to investigate how to reduce the consumption of Si during the silicide formation while keeping the excellent electrical and thermal stability of the epitaxial silicide.

In this paper we report our efforts on adding amorphous silicon layer in Co/Ti layer for reduction of the Si consumption in shallow junction. It was found that epitaxial $CoSi_2$ can be formed by Co/Si/ Ti/ Si (100) reaction. By varying the thickness of Si layer, its effect on the growth and self-aligned process was investigated.

Experiments

N-type Si (100) wafers with resistivity of 5-8Ω•cm were used as starting substrates. 500nm SiO_2 was thermally grown on some wafers for selective etching experiment. The ion beam sputtering technique was applied for metal deposition. Following a standard RCA cleaning process and short-time dipping in a diluted HF solution, the wafers were load into an oxford sputtering system equipped with Ti, Co, and Si targets. The chamber was evacuated to a base pressure of 2×10^{-7} torr and then back filled with high purity argon. By rotating the target holder, Ti, Co, Si films were deposited sequentially by Ar^+ beam sputtering under an argon pressure of 5×10^{-5} torr. The film thickness was on-line monitored by a quartz crystal oscillator. The thickness of Co and Ti was fixed at 15nm and 3nm, while the thickness of α-Si was varied from 4nm to 15nm.

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Rapid thermal annealing was applied for the silicidation. One step annealing or two step annealing was applied. In the one step annealing, samples were directly annealed to certain temperature and in the two step annealing, samples were first annealed at certain temperature between 600~900°C, then after selective etching the unreacted Co and Ti, they were re-annealed at a higher temperature. Different selective etching solution were applied for test of their selectivity on SiO_2/Si substrate.

The film phase and structure were characterized by x-ray diffraction(XRD) using Cu Kα1 radiation, cross-sectional transmission electron microscopy (XTEM) and Rutherford backscattering spectrometry(RBS) using 2MeV He^+ ions at either random or aligned (channeling) incidence with a back-scattering angle of 165°. The ternary silicide was removed in a buffered HF solution before RBS measurement. A four-point probe was used to measure the sheet resistance and thermal stability of the formed films.

Results and Discussion

The solid phase reaction of Co/Si/Ti/Si multilayer after annealing at various temperatures was investigated by X-ray diffraction measurement. Fig.1(a) and (b) show the XRD spectra of the samples after annealing at 750°C and 1000°C for 1 minutes respectively. After annealing at 750°C, the dominant diffraction peaks of $CoSi_2$ from the same lattice phase as Si(100) have appeared with a small peak of $CoSi_2$(220). It indicates that annealing at 750°C has produced a thin epitaxial $CoSi_2$ film on Si(100) while with a little amount of mis-oriented grains. When carefully observed, a low broad peak with the d value of 0.199nm matching the JCPDS data for Co_2Ti_4O can be found. Recently, Selinder et.al have studied the Co/Ti/Si solid phase reaction using in-situ XRD technique. They found that during annealing in a certain temperature range, a transient compound which is called M phase by them is formed[6]. The M phase is a kind of ternary compound of Co, Ti and O. It can be $CoTi_2O_4$ or $CoTiO_3$ with a structure of cubic spinel. The ternary compound can act as a diffusion barrier in the solid phase reaction. In our experiment, a ternary compound of Co_2Ti_4O is observed. After high temperature annealing of 1000°C, only the series of (100) diffraction peaks of $CoSi_2$ are detected.

With the interposed Si thickness varying from 4nm to 12nm, the XRD spectra of the samples after 1000°C thermal annealing show no obvious changes. They all show sharp peaks of (100) series of $CoSi_2$, which indicates the epitaxial characteristic. Yet when the added Si layer was 15nm, a very small $CoSi_2$(220) peak appeared in the XRD spectrum of the $CoSi_2$. Shown in Fig. 2, which indicates there are a few of nonepitaxial grains in the $CoSi_2$ layer.

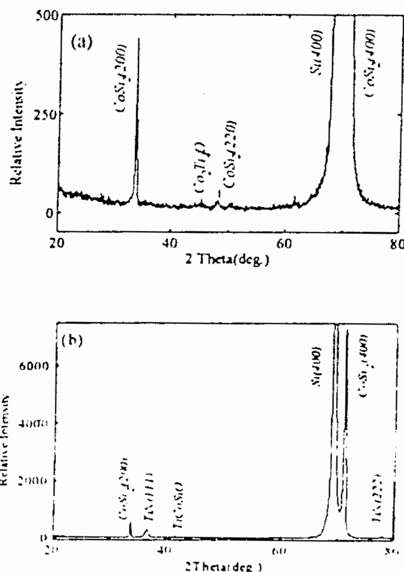

Fig.1 The XRD spectra of Co(15nm)/Si(4nm)/Ti (3nm) / Si(100) after annealing at (a) 750°C; (b) 1000°C for 1 minute in N_2 atmosphere.

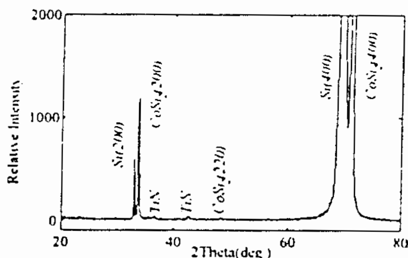

Fig. 2 The XRD spectrum of Co(15nm) /Si(15nm) / Ti(3nm)/Si(100) after two step annealing, that is, 650°C/1min + S.E.+1100°C/10s.

The epitaxial quality of $CoSi_2$ was investigated by RBS channeling. Fig.3 is the random and aligned RBS spectra of $CoSi_2$/Si (100) formed from Co(15nm)

/Si(4nm)/Ti(3nm)/Si(100) after removal of the surface TiN and ternary silicide. The prominent channeling effect in the aligned spectra indicates the epitaxial growth of $CoSi_2$ films on Si(100). The channeling yields minimum(χ_{min})of Co signals of $CoSi_2$ are 5.2%.

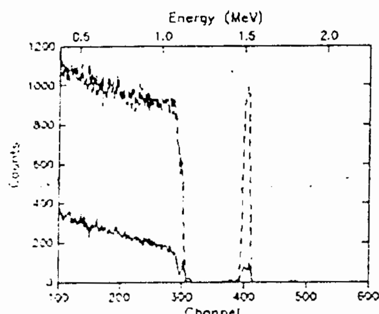

Fig. 3 The RBS random and aligned spectrum of Co(15nm)/Si(4nm)/Ti(3nm)/Si(100) after two step annealing. The surface TiN and ternary compound have been removed.

RBS results show that, within a certain thickness range for the added Si, the Si affects little on the epitaxial quality of $CoSi_2$. When the thickness of added amorphous Si is increased to 6nm, the χ_{min} of $CoSi_2$ is about 7%. We found in our thickness range of the added Si, all the film show the prominent channeling effect. Yet the thicker the added Si layer, the larger the channeling yield minimum

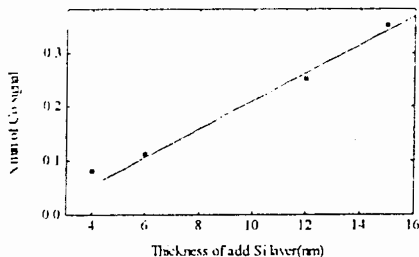

Fig. 4 The channeling yield minimum of $CoSi_2$ calculated by integration method vs. the Si thickness in Co/Si/Ti/Si structure.

The relation between χ_{min} of Co signal and the thickness of added Si layer is plotted in Fig. 3. It is interesting to find that they have a linear relationship when the Si thickness is larger than 6nm.

When the added Si layer is thicker, that is the atomic ratio of Si to Co becomes larger, the Co will not only react with substrate Si to form epitaxial $CoSi_2$, it will also react with added Si to form nonepitxial $CoSi_2$. Thus the χ_{min} will become larger. So there may be an optimum thickness of α-Si layer for good epitaxy.

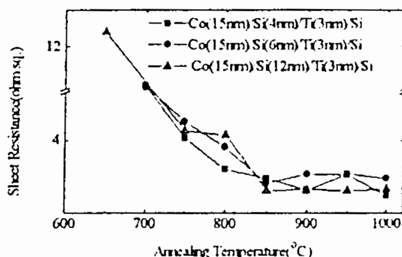

Fig. 5 The sheet resistance variation of Co/Si/Ti/Si structure with annealing temperature for 1min.

The sheet resistance of Co/Si/Ti/Si structure with different thickness of added Si after isochronical thermal annealing at different temperature for 1min was shown in Fig.5. No significant difference can be found in the annealing behavior of these film. All the films have excellent thermal stability. The film obtained from Co(15nm)/Si(4nm)/Ti(3nm)/Si(100) annealing at 1000°C for 1 minute has a minimum sheet resistance value of 2.9Ω/□. The thickness of the $CoSi_2$ film measured from the TEM micrograph is about 46nm, so the resistivity of $CoSi_2$ formed by this method is about 14μΩ•cm.

The micro-structure of the formed $CoSi_2$ was observed by XTEM. Fig.6 shows the XTEM of Ti(3nm)/Co(15nm)/Si(4nm)/ Ti(3nm)/Si(100) after two step annealing . The insert on the up-right corner was the selected area electron diffraction pattern of $CoSi_2$ along [110] zone axis. It shows that $CoSi_2$ has flat interface with Si. The film also has flat surface, which is due to the two step annealing. The $CoSi_2$ layer is homogenous without grain boundary, indicating the film has excellent crystallinity. When one carefully observes the $CoSi_2$/Si interface, a few (111) facets were seen at the interface. Because $CoSi_2$(111) has lower surface energy than $CoSi_2$(100), the (111) facets tend to form to lower the whole system energy.

To test the applicability of this method in VLSI technology, selective etching experiments on both oxide wafer and pattered wafers were carried out. The results on oxide wafer show that using a proper selective solution and procedure, the unreacted Co, Ti and Co_2Si can be

removed even the amorphous Si layer is as thick as 15nm. By comparing the $H_2SO_4+H_2O_2$, $HCl+H_2O_2$, $NH_4OH + H_2O_2$ solution, we found that the $NH_4OH+H_2O_2$ solution is the most effective selective solution for removing the Co_2Si phase. The SEM photograph of a 1μm patterned CMOS wafer(Fig.7) shows that under proper annealing procedure and selective etching, fully self-aligned silicide film can be formed on both source/drain and poly gate regions with no lateral growth.

SUMMARY

The solid reaction of Co/Si/Ti/Si multilayer was investigated for reduction of Si consumption in junction region. XRD, RBS, TEM show that excellent epitaxial $CoSi_2$ film has grown on Si(100) wafer by Co/Si/Ti/Si solid reaction. The effect of added amorphous Si layer on the epitaxial growth of $CoSi_2$ and Self-aligned process was investigated. RBS shows that with α-Si layer of certain thickness an epitaxial $CoSi_2$ thin film with very low channeling yield minimum can be obtained. The SEM shows that by proper thermal annealing and selective etching procedures, a self-aligned silicided MOS device structure can be formed by the Co/α-Si/Ti/Si(100) multilayer.

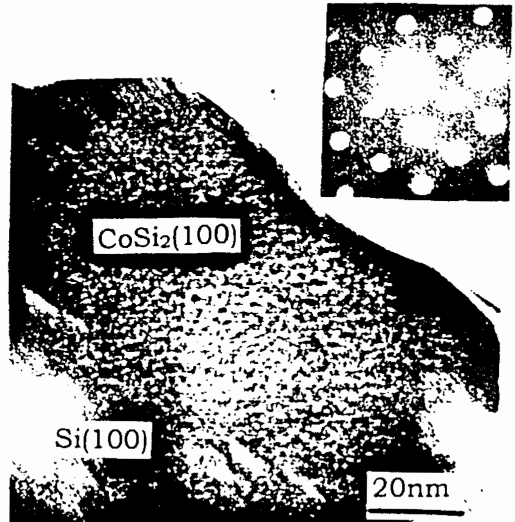

Fig. 6 The XTEM of Ti(3nm)/Co(15nm)/ Si(4nm) / Ti(3nm)/ Si(100) after two step annealing. The insert on the right is the electron diffraction of $CoSi_2$ along <110> zone axis.

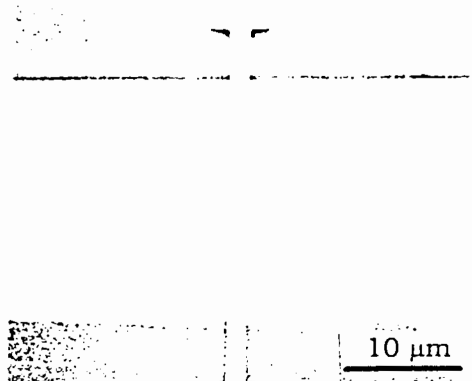

Fig. 7 The SEM photograph of 1μm patterned CMOS wafer after two step silicidation by Co(15nm)/Si(4nm)/ Ti(3nm) /Si(100) reaction.

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