# SYMPOSIUM E

# Low-Dielectric Constant Materials and Applications in Microelectronics IV

April 14 - 16, 1998

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* Invited paper

SESSION E1: LOW-k OXIDES AND GLASSES
Chair: Chien Chiang
Tuesday Morning, April 14, 1998
Pacific H

**8:30 AM *E1.1**
OVERVIEW OF PROCESS INTEGRATION AND RELIABILITY ISSUES FOR LOW K DIELECTRICS IN ADVANCED MULTILEVEL INTERCONNECTS. R.H. Havemann, M.K. Jain, W-Y. Shih, C. Jin, R.S. List, A.R. Ralston, M.C. Chang, E.M. Zielinski, G.A. Dixit, A. Singh, S.W. Russell, J.F. Gaynor, and A.J. McKerrow, Silicon Technology Development, Texas Instruments, Inc., Dallas, TX.

The era of silicon Ultra-Large-Scale-lntegration has spurred an ever-increasing level of functional integration on-chip, driving a need for greater circuit density and higher performance. While traditional transistor scaling has thus far met this challenge, Interconnect scaling has become the performance- limiting factor for new designs. Both interconnect resistance and capacitance play key roles in overall performance, but modeling simulations have highlighted the importance of reducing parasitic capacitance to manage crosstalk, power dissipation and RC delay. New materials with lower permittivity are needed to meet this challenge. This paper will summarize the process integration and reliability issues associated with the use of novel low k materials in multilevel interconnects.

**9:00 AM E1.2**
LIQUID-PHASE DEPOSITION OF LOW-k ORGANIC SILICON-OXIDE FILMS. Kouichi Usami, Kazuhito Sumimura, Satoshi Sugahara and Masakiyo Matsumura, Tokyo Institute of Technology, Dept of Physical Electronics, Tokyo, JAPAN.

We have studied liquid-phase deposition1) of low-k silicon-oxide films from $CH_3Si(OC_2H_5)_3$ solution at room temperature. We added a small amount of $NH_4OH$ and HCOOH in $H_2O$ for acceleration of chemical reactions, and also ethylene glycol for surfactant. AES spectrum for the as-deposited film indicated that the film had predominantly Si, O and C with their composition ratio of 1: 1.5: 1. FTIR spectrum showed strong absorption peaks at 1280cm$^{-1}$ and 780cm$^{-1}$ and also at 1050cm$^{-1}$, indicating that dominant chemical bonds were Si-$CH_3$ and Si-O. XPS spectrum indicated that almost all Si atoms bond with three O and one $CH_3$. Incorporation of dense $CH_3$ groups resulted from the chemical property that $H_2O$ can break Si-$OC_2H_5$ bonds but not Si-$CH_3$ bonds. The Si-$CH_3$ bond remained in the film even after annealing at 600ºC. Dielectric constant, low-field (=100kV/cm) resistivity and breakdown field-strength (at 1?A/

metals on virgin polymer surfaces deviate markedly from unity. Diffusion into the polymer increases strongly at low deposition rates, where a large fraction of isolated metal atoms is able to diffuse into the polymer before being trapped by other atoms at or near the surface. No significant diffusion is expected from a continuous metal film as a consequence of the high cohesive energy of the metal. The model emerging from these observations allows us to predict the salient features of interface formation between metals and polymers in general and particularly with respect to the new low-k polymers.

**11:00 AM E1.7**

RELATION AMONG THE FILM PROPERTIES, STRUCTURE AND PROCESS OF F-DOPED SILICON DIOXIDE FILMS. SangWoo Lim, Yukihiro Shimogaki, Yoshiaki Nakano,*, Kunio Tada*, and Hiroshi Komiyama, Univ of Tokyo, Dept of Chemical System Engineering, *Dept of Electronic Engineering, Tokyo, JAPAN.

We studied the reduction mechanism of the dielectric constant of F-doped silicon dioxide films. From the estimation of the dielectric constant at each frequency using CV measurement, Kramers-Kronig relation and the square of the refractive index, we suggest that the dielectric constant due to ionic and electronic polarization is not the dominant factor in decreasing the dielectric constant. It is important to remove OH in films to obtain very low dielectric constant F-doped silicon dioxide films, because Si-OH is the main factor of the orientational polarization in silicon oxide films made by PECVD. To investigate the reaction mechanism which controls the film structure, we changed the residence time of gas in chamber by varying the flow rate. When the residence time in chamber decreases, the film deposition rate increases. We tried to explain flow rate dependency of the deposition rate using a simple CSTR (continuous stirred tank reactor) model. It can be concluded that SiH4 directly reacts at the surface to deposit the film, and the deposition path through the intermediate can be negligible in our PECVD system. Step coverage analysis using test structure or trench was also carried out to examine the surface chemistry.

**11:15 AM E1.8**

NEWLY DEVELOPED LOW-K AND LOW-STRESS FLUORINATED SILICON OXIDE UTILIZING TEMPERATURE-DIFFERENCE LIQUID-PHASE DEPOSITION TECHNOLOGY. Ching-Fa Yeh, Yueh-Chuan Lee and Su-Chen Lee, Department of Electronics Engineering & Institute of Electronics, National Chiao-Tun University, Hsinchu, Taiwan, CHINA.

To meet the requirements of low-K and low-stress intermetal dielectric (IMD) for future ULSI devices, a novel temperature-difference liquid-phase deposition (TD-LPD) method is proposed. The deposition solution of supersaturated silicic acid with high concentration of fluorine can be achieved by raising deposition temperature larger than 15?C from dissolution temperature (0?C). Therefore, TD-LPD SiOF as an IMD is expected to have excellent properties.
In this study, the excellent properties like deposition rate, fluorine concentration, dielectric constant, stress and the reliability issues are verified. The deposition rate increases exponentially from 30 to 700 A/hr with temperature difference increasing from 15 to 35?C. For TD-LPD SiOF film deposited at 25?C, the fluorine concentration determined by X-ray photoelectron spectroscopy is 6.46 A.C.%. The dielectric constant (K) and the stress are as low as 3.40 and 32MPa tensile, respectively. The reliability problems of TD-LPD SiOF are also investigated in terms of thermal stability and moisture resistance. After 400?C annealing in N2 ambient, the dielectric constant further decreases to 3.34 due to removal of OH bonds. The thermal stability can be up to ?700?C, beyond which the K value becomes increased due to escape of fluorine. The stability obviously shows sufficient for TD-LPD dielectric applied as an IMD. As for moisture resistance, after TD-LPD SiOF being stressed in boiling water for 1 hour, its dielectric constant only increases slightly to ?3.45. Generally an IMD is required to endure repeated cycles of thermal annealing and moisture stress. The K value and the electrical properties less vary in the second cycle in comparison with the first cycle. A feasible mechanism describing the less variation is first proposed.

**11:30 AM E1.9**

LOW-DIELECTRIC CONSTANT $SiO_2$ FILMS FOR ULSI INTERCONNECTIONS PREPARED BY $CF_4$. Shu Qin, Yuanzhong Zhou, and Chung Chan, Plasma Science and Microelectronics Laboratory, Northeastern University, Boston, MA; Paul K. Chu, Department of Physics & Materials Science, City University of Hong Kong, Kowloon, HONG KONG

The multilevel interconnections have been used in ultra-large-scale integrated circuits (ULSI). To minimize the crosstalk and RC time delay, it is necessary to keep interlayer dielectric capacitance low. This can be implemented through the introduction of low-dielectric constant interlayer films. The properties and the fabrication techniques of the interlayer dielectrics have to meet the following requirements: (1) a low dielectric constant, (2) good electrical and mechanical properties, (3) a high planarization and narrow gap filling capability, and (4) a low process temperature. So far, the existing techniques cannot satisfy all of the above requirements due to the limitations of the physical mechanisms. Plasma ion implantation (PII) doping technique has been utilized to prepare the low-dielectric constant (low k) $SiO_2$ films as the high quality interlayer dielectrics for ULSI applications. The $SiO_2$ films are fluorinedoped/carbondoped by PII with $CF_4$ plasma in an ICP plasma reactor. The dielectric constant of $SiO_2$ films was significantly reduced from 4.10 to 3.50 after 5 minute PII. An analysis of a double layer model indicates that a high quality dielectric layer with a dielectric constant down to 2.8 can be achieved by an optimized PII process. Contrasting to other conventional low-k material techniques, PII process also consistently improve other electrical properties of $SiO_2$ films such as bulk resistivity and dielectric field breakdown strength. The etching effect of $CF_4$ PII may be beneficial to planarization and gap filling of dielectric interlayers.

**11:45 AM E1.10**
POROUS ALUMINA AS LOW-K MATERIAL FOR INTERCONNECT DIELECTRIC. S.Lazarouk, P. Jaguiro, S. Katsouba, Belarusian State University Informatics and Electronics, Minsk, BELARUS.

Improvements in electronics require increased speed, decreased dimensions. But as dimensions decrease interconnect problems are the most severe limiting factor in IC. Interconnect delay can be minimized by using low-dialectric constant materials for interconnect dielectric. In order to replace SiO2 with low-k material based on porous alumina we have developed the technology of in-built aluminum interconnects based on electrochemical Al anodization processes. In our technology aluminum, which is between the inerconnect line, is converted in to oxide by using porous electrochemical anodization. Thus we obtain aluminum lines, which are in-built in porous alumina. By using the special regimes of anodization we have obtained the dielectric constant value in the range 3.0 - 4.0. The relief step height for one interconnect level is less than 0.2 mm for 1.0 mm-thick Al films. The process of porous anodization allows to obtain planar surface by using this process for each layer of interconnects and interlevel insulation with in-built contact pillars. The developed processing technique has been tested for CMOS submicron technology.

## SESSION E2: POLYMERIC AND INORGANIC LOW-k MATERIALS
Chair: Toh-Ming Lu
Tuesday Afternoon, April 14, 1998
Pacific H

**1:30 PM *E2.1**
EVALUATION OF LOW DIELECTRIC CONSTANT MATERIALS FOR INTER-LEVEL DIELECTRIC APPLICATIONS. Huei-Min. Ho*, Robert J. Fox, Sematech, Austin, TX. *on assignment from Intel Corporation.

In the last few years, research and development activities on low k dielectric materials for inter-level dielectric applications have increased significantly. Numerous materials at various dielectric constant levels, e.g., k<4.0, k<3.0, k<2.5, and k<2.0, have been proposed and many of them have been evaluated at SEMATECH. The approaches taken at SEMATECH for low k material evaluation include: a) material property characterization, b) one- and two-level metal module evaluation with Al/RIE architecture, and c) one- and two-level metal module evaluation with Cu/Damascene architecture. In this paper, the characterization techniques developed for low k material evaluation, along with data collected, will be presented. Current techniques have mainly targeted spin-on polymer materials, and the need to develop advanced techniques for on-wafer and porous material measurements have become imminent. Module evaluation includes physical observations and electrical testing. It has demonstrated that low k materials can be successfully integrated into back-end-of-line (BEOL) processes with sound structural and electrical integrity. The results, using Al/RIE architecture, have shed light upon the validity of some typical concerns of low k material properties, such as $T_g$, fluorine content, etc. Electrical tests have also proven sensitive to issues associated with low k material integration. Representative results of module evaluation and achieving low k BEOL integration will also be discussed.

**2:00 PM E2.2**
PHASE SEPARATION OF BEHAVIORS OF POLYIMIDE BLENDS. Chul Hae Ryu and Young Chan Bae, Hanyang Univ, Dept of Industrial Chemistry, Seoul, KOREA.

The industry has recognized the need of developing low dielecrtic materials and developed various low dielectric materials. Low dielectric constant interlayer(ILD) materials are required for the advanced silicon integrated electronics such as those in the ultra large scale integration(ULSI) era. As minimum features are reduced to the micron and submicron range, line width control over high steps and different parts of the wafer topology becomes increasingly difficult. With the increase in the integration of electronic devices, and the need to reduce overall sizes, companies are now moving to multilevel metalization. Some of the current materials and processing technologies are unable to overcome the difficulties for the production of the next multilevel of integrated circuits where higher speed and density are demanded. Many researchers have studied and focused on low dielectric polymer films in order to overcome the difficulties of high density. Polyimides and polyimide blends have been the most concerning materials of them and studied in many cases. Polyimides and polyimide blends have some desired properties which include low dielectric constants, low moisture absorption,

# LOW-DIELECTRIC CONSTANT SiO(F,C) FILMS FOR ULSI INTERCONNECTIONS PREPARED BY $CF_4$ PLASMA ION IMPLANTATION

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## ABSTRACT

Plasma ion implantation (PII) doping technique has been utilized to prepare a new low-dielectric constant (low k) material SiO(F,C). Fluorine and carbon were implanted into $SiO_2$ films by $CF_4$ PII using an ICP plasma reactor. The effective dielectric constant of the films was significantly reduced after PII doping. An analysis of a double layer model indicated that a high quality dielectric layer with a dielectric constant down to 2.8 can be achieved by an optimized PII process. Contrasting to other conventional low-k material techniques, PII process also improved bulk resistivity and electrical field breakdown strength. The improvement possibly resulted from adding carbon into the films. The etching effect of $CF_4$ PII could be beneficial to planarization and gap filling of dielectric interlayers.

## INTRODUCTION

One of the major trends in modern microelectronics is that device dimensions has kept shrinking. As the device size shrinks to less than 0.25 µm, significant RC delay, power consumption, and crosstalk noise will be caused by the resistance-capacitance coupling of the interconnect system[1]. To address these issues, it is necessary to introduce low dielectric constant (low k) materials as the interlayer dielectric. For sub-0.5-µm devices, low k materials must meet stringent requirements on the electrical, chemical, mechanical, and thermal properties. Besides low dielectric constant, these requirements include low leakage current, high electrical field strength, low moisture absorption, no metal corrosion, low residual stress, high thermal stability, high thermal conductivity, and high gap filling capability, *etc.*[2]. There are a wide variety of low k materials under development. Currently no single materials can meet all requirements. For example, the polymers, which k values are in the range of 2-3, suffer from problems including poor thermal stability, low thermal conductivity, and difficulty in process integration. Fluorinated amorphous carbon films, which k values are around 2.5, have little mechanical strength and are not resistant to oxygen-plasma exposure[3].

Silicon dioxide has long been used as interlayer dielectric because of its good properties and compatibility in the semiconductor processing. It is well known that doping silicon dioxide with fluorine can reduce its dielectric constant. The higher fluorine concentration results the lower dielectric constant. The fluorine is usually incorporated into dielectrics during the films are deposited by plasma enhanced CVD (PECVD) or high density plasma CVD (HDP-CVD)[4,5]. However, the dielectric constant of the fluorinated $SiO_2$ films is difficult to be lowered to 3.5 by CVD processes without significantly degrading its chemical and other properties[6]. The electrical and mechanical properties of the $SiO_2$ films are usually degraded by the fluorine doping. For example, the bulk resistivity and breakdown field strength of $SiO_2$ are reduced after fluorine is added to the materials. The additional use of carbon doping to achieve both a lower dielectric constant and improved film stability has been reported[7]. The CVD processes only allow a small amount of carbon to be incorporated into $SiO_2$ films when adding fluorine to the films. For example, adding $C_2F_6$ to conventional tetraethoxysilane (TEOS)-based PECVD deposition, fluorine content up to 14 at.% in the films could be achieved, but carbon concentration is less than 0.1 at.%[4].

Plasma ion implantation (PII) is a niche doping technology that has been utilized to semiconductor applications and materials modification[8,9]. In PII process, the substrate to be implanted is immersed in a plasma and biased to a negative sequence. The ions in the plasma are accelerated by the sheath voltage and implanted into the substrate. The primary features of PII include high dose rate independent of the implantation area ($10^{16}/cm^2$ sec), minimum charging effect, low equipment cost, uniform doping for non-planar samples, and co-implantation of multiple species. These characteristics make PII a suitable low-cost technique for large area processing and synthesis of new materials.

In this paper, the preparation of a new low k material SiO(F,C) as the high quality interlayer dielectrics for ULSI applications by PII doping technique is presented. The films were formed by implanting fluorine and carbon into $SiO_2$ films by PII technique with $CF_4$ plasma in an ICP plasma reactor. The capability of multiple species implantation allows fluorine and carbon be introduced into $SiO_2$ films simultaneously. Low k dielectric films with good quality including lower dielectric constant and higher bulk resistivity and breakdown field strength have been achieved.

## EXPERIMENTS

An inductively-coupled plasma (ICP) system was used for the PII low k material experiments. It consists of a chamber with a multipolar magnetic confinement structure, an electrical system to transmit 13.45 MHz RF power into the chamber, and a wafer holder connected to a high voltage pulse generator. A flat pancake-type coil is placed outside the chamber on top of a 3/4 inch thick, 9 inch diameter quartz window. ICP source has many advantages over other conventional plasma sources, including higher ion density, lower working pressure, and better radial ion density uniformity which is critically important to the ULSI applications.

The $CF_4$ plasma was characterized by a Langmuir probe. Fig. 1 shows the ion density at 20 cm below the quartz window versus working pressure when ICP RF power is 700 watts. Typical $CF_4$ plasma parameters for this experiment are: plasma density $i_n \approx 10^{11}\ /cm^3$, electron temperature $T_e \approx 4$ eV, and plasma potential $V_p \approx 30$ V.

P-type single-crystalline <100> Si wafers with $\rho$ = 2-20 Ω-cm were used as starting material. A 2500 Å-thick $SiO_2$ film was grown on each Si surface by a routine thermal oxidation process. Then PII with $CF_4$ plasma was performed to implant F and C into the $SiO_2$ to form ISO(FMC) films. The process conditions were as follows: base pressure $<10^{-6}$ Torr, working pressure 0.2 to 0.7 mTorr, gas flow rate ~12 sccm, RF power 700 W, pulse voltage -2 to -5 kV, pulse repetition frequency (prf) 10 kHz, pulse width 2 μsec, and samples were cooled to room temperature. After PI process, a 2000 Å-thick Al layer was deposited on the surface by E-gun evaporation and Al/$SiO_2$/p-Si structures were formed by lithography. Afterwards, a post-implant annealing process was performed in $N_2$ gas at 385 °C for 20 minutes.

The circular capacitors with two different areas, $1.782\times10^{-3}$ $cm^2$ and $1.208\times10^{-4}$ $cm^2$, were measured with a HP 4277A LCD meter. The dielectric constant of the films was calculated from the maximum capacitance values in the C-V measurement at 1 MHz. The bulk leakage current and breakdown field strength of the $SiO_2$ films were measured with a HP 5155A semiconductor parameter analyzer and a curve tracer. The resistivity of the films was calculated

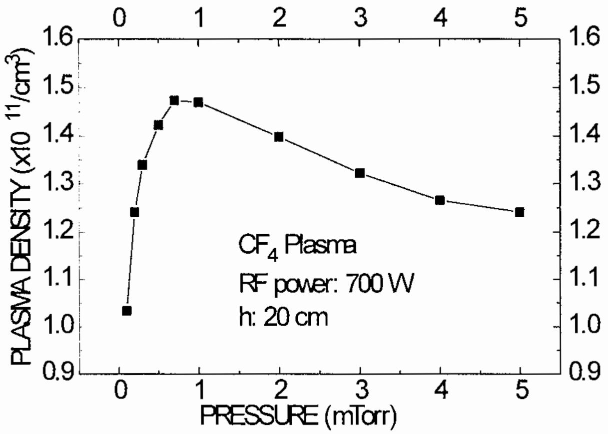


**Fig. 1** Ion density vs. working pressure, RF power: 700 W, the position is 20 cm below the quartz window

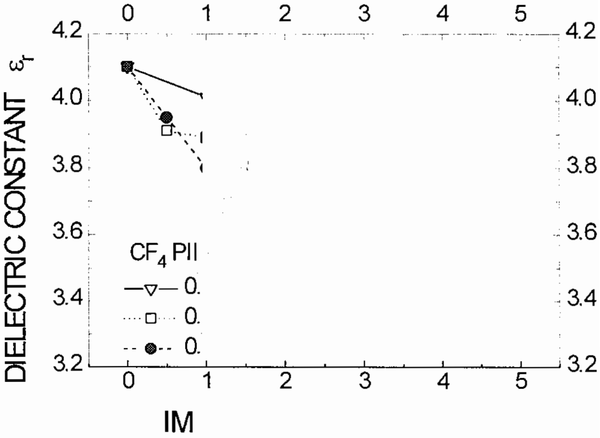


**Fig. 2** The effective k values vs. process time. (ICP RF power: 700 W, Ion density: $1.25\times10^{11}/cm^3$, Pulse: -2 kV, $t_p$ 2 μsec, prf 10 kHz, Annealing: 20 min in $N_2$ at 385 °C).

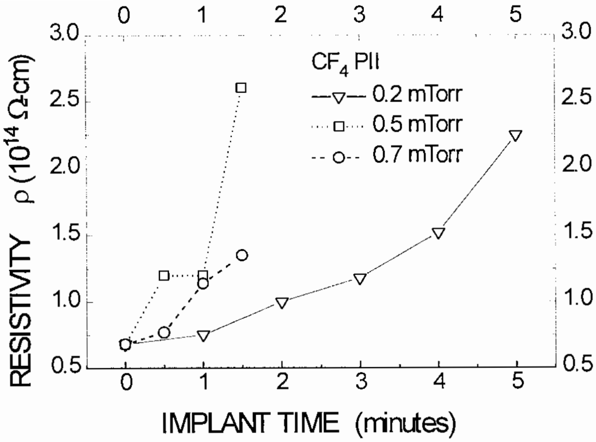
based on the measurements of the leakage current and the dimension of the capacitors and the thickness of the dielectric films. The thickness and refractive index of $SiO_2$ films were measured by an ellipsometer (GAERTNER-L117) and a Dektak profilometer (Veeco-Sloan 8000). Since the atomic composition of films was not uniform throughout the depth, most data obtained from the measurement are effective ones.

## RESULTS AND DISCUSSION

Table I gives the major measured properties of the SiO(F,C) films for different PII process time when the working pressure is 0.2 mTorr. The dielectric constant, k, monotonously decreases from 4.10 to 3.50 when the process time is 5 minutes. Besides the reduction of the dielectric constant, PII also improves bulk resistivity and breakdown field strength in contrast with other low k processes. One interesting feature of SiO(F,C) was that there is no big change of the refractive index of the film, which was kept constant at about 1.46. Other low k processes indicated lower refractive index when the F concentration in the dielectrics was high [5]. These unique features of SiO(F,C), including improved resistivity and breakdown field strength and constant refractive index, possibly resulted from the addition of carbon. Table I also shows the etching observed in $CF_2$ PII doping experiment. The etching rate was 283 Å/min. The films processed at 0.5 mTorr and 0.7 mTorr demonstrated similar properties as that at 0.2 mTorr. The etching rates for 0.5 and 0.7 mTorr processes were 680 and 946 Å/min., respectively.

Fig. 2 shows the evolution of the effective dielectric constant of SiO(F,C) films versus PII process time for the different working pressures. Fig. 3 shows the evolution of the effective resistivity of $SiO_2$ films versus PII process time. Fig. 4 shows the evolution of the breakdown field strength of $SiO_2$ films for different PII process time. The improvement on the effective values of the material properties varied at different working pressures.

Figs. 5 (a) and (b) display SIMS profiles of F and C in the SiO(F,C) films when the pressures were 0.2 and 0.5 mTorr, respectively. SIMS data shows that a large amount of carbon and fluorine were incorporated into the $SiO_2$ films. The dose ratio of carbon to fluorine is higher



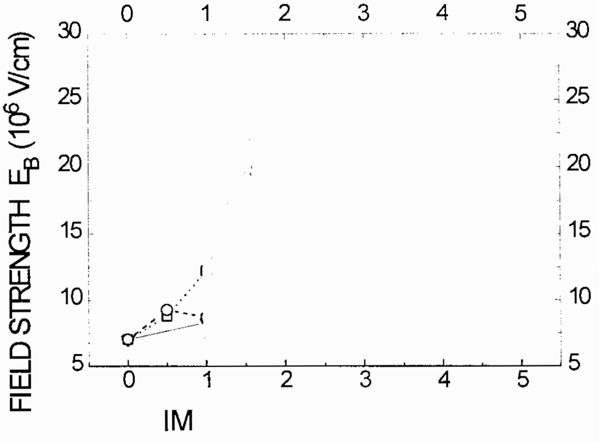


**Fig. 3** The effective resistivity of SiO(F,C) films versus the PII process time. (ICP RF. power: 700 W, ion density: $1.25\times10^{11}/\text{cm}^3$, pulse: -2 kV, $t_p$ 2 μsec, prf 10 kHz, annealing: 20 min in $N_2$ at 385 °C)

**Fig. 4** Th effective breakdown strength of SiO(F,C) films vs. the PII process time. (ICP RF power: 700 W, ion density: $1.25\times10^{11}/\text{cm}^3$, pulse: -2 kV, $t_p$ 2 μsec, prf 10 kHz, annealing: 20 min in $N_2$ at 385 °C)

**Table I.** Major properties of $SiO_2$ films before and after PII. (Pressure: 0.2 mTorr, ICP RF power: 700 W, Pulse: -2 kV, $t_p$ 2 μsec, prf 10 kHz, annealing: 20 min in $N_2$ at 385 °C)

| | Before treatment | 1 min | 2 min | 3 min | 4 min | 5 min |
|---|---|---|---|---|---|---|
| $\varepsilon_r$ | 4.10 | 4.01 | 3.89 | 3.86 | 3.78 | 3.50 |
| ρ ($10^{14}$ Ω cm) | 0.68 | 0.75 | 1.00 | 1.18 | 1.52 | 2.24 |
| $E_{Break}$ ($10^6$ V/cm) | 7.02 | 8.32 | 8.52 | 13.09 | 8.81 | 17.12 |
| Thickness (Å) | 2564 | 2343 | 1907 | 1700 | 1591 | 882 |
| Refractive Index | 1.460 | 1.441 | 1.466 | 1.464 | 1.465 | 1.461 |

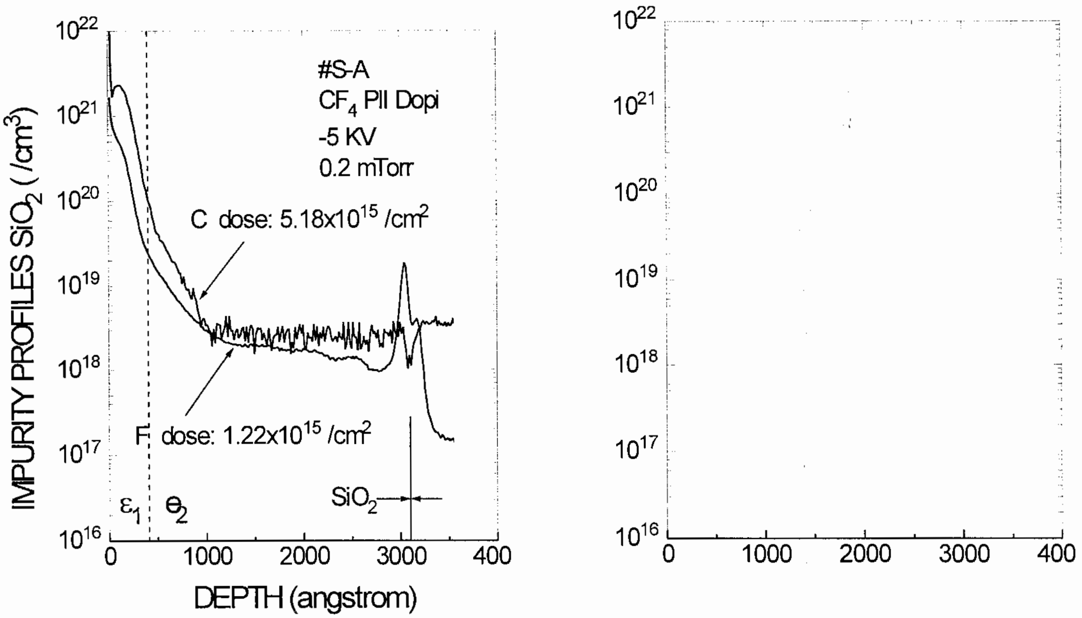
0.5 mTorr (10) than 0.2 mTorr (4.2). SIMS data also shows that the processed films have non-uniform profiles of F and C. Fluorine and carbon were implanted into the top layer of the films.

A double layer model (Fig. 6) was used to estimate dielectric constants in the implanted layer. The boundary was chosen at 300 Å below the top surface, as shown as the vertical dash line in Fig. 5. With this model, we have following equations.

$$C = \frac{\varepsilon_{eff} A}{d_1 + d_2}, \qquad C_1 = \frac{\varepsilon_1 A}{d_1}, \qquad C_2 = \frac{\varepsilon_2 A}{d_2} \qquad \text{(1 a, b, c)}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \qquad (2)$$

where $d_1$=300Å is the thickness of the implanted layer, $d_1+d_2$ is the total thickness of the dielectric film, and A is the area of the capacitors. Solving (1) and (2) yields



(a) (b)

**Fig. 5** SIMS profiles of F and C in SiO$_2$ film after 0.2 mTorr (a) and 0.2 mTorr (b) CF$_4$ PII.

$$\varepsilon_1 = \frac{d_1 \varepsilon_2 \varepsilon_{eff}}{\varepsilon_1 (d_1 + d_2) - \varepsilon_{eff} d_2} \tag{3}$$

Then, the k values of the implanted layer were extracted, which are shown in Fig. 7. The results demonstrated that the k value as low as 2.8 had been achieved. Unlike the effective values, the extracted dielectric constants in the implanted layer seem saturate after a short time PII.

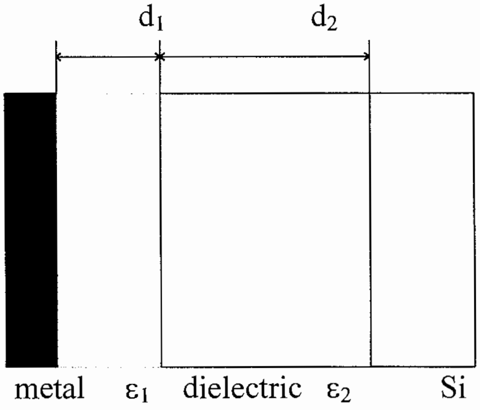


**Fig.6** Double layer model. d$_1$: the implanted layer; d$_2$: undisturbed SiO$_2$

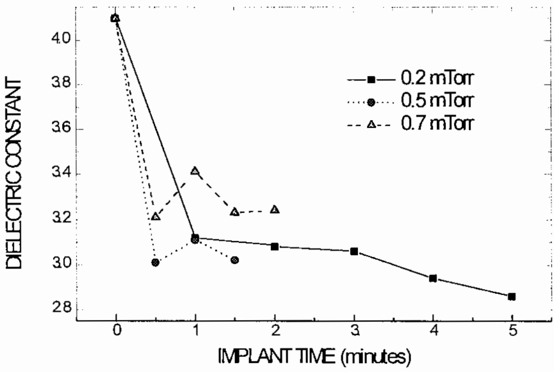


**Fig.7** The extracted k values vs. PII process time. d$_1$ =300Å, k$_2$=4.1

Etching phenomena could play an important role in PII SiO(F,C) synthesis. Etching can cause the retained doses reduced and saturate during PII process[10], which in turn result the saturation of film improvement. Etching consumes fluorine and change fluorine content in the films. A higher etching rate was observed at higher pressure, which led higher ratio of carbon to fluorine in the films. Etching could be beneficial to planarization and gap filling of dielectric interlayers. Integrated into semiconductor fabrication using a Dep-PII-Dep-PII.... sequence, the PII approach presented here could produce optimal results of the low k and planarization purposes.

## CONCLUSION

Plasma ion implantation (PII) doping technique has been investigated as a novel approach to prepare the low-dielectric constant (low k) SiO(F,C) films as the high quality interlayer dielectrics for ULSI. SiO(F,C) films have demonstrated great reduction of the dielectric constant. With an optimal PII process condition: 0.2 mTorr pressure, -2 kV pulse potential, 2 μsec pulse width, and 10 kHz pulse repetition frequency, the dielectric constant was significantly reduced from 4.1 to 2.8 in the implanted layer and other electrical parameters such as the bulk resistivity and dielectric breakdown field strength were also improved. Superior quality of the low k dielectrics possibly resulted from the large amount of carbon that was incorporated into the SiO(F,C) films by $CF_2$ PII. The process also promises good gap filling capability.

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